# High Power Positive Hot-Swap Controller with Power Monitor via PMBus

## FEATURES

- Wide operating voltage range: 8.5 V to 80 V
- Monitors currents, voltages, and power with ADC
- Adjustable, 5% accurate current limit: 6 mV to 20 mV
- Current foldback limits MOSFET power dissipation for overstress protection
- Monitors $V_{GS}$ and $V_{DS}$ for MOSFET health
- Peak detect registers for current, voltage, and power
- Reports input or output power
- Remote temperature sensing with programmable warning and shutdown thresholds
- ±1% accurate, 12-bit ADC for $I_{OUT}$, $V_{IN}$, and $V_{OUT}$
- Available in 39-lead, 7 mm x 7 mm, QFN package

## APPLICATIONS

- High availability server backplane systems
- 12 V/24 V/48 V/54 V Distributed power systems
- Industrial

## GENERAL DESCRIPTION

The LTC4286 is an integrated solution for hot-swap applications allowing a board to be safely inserted and removed from a live backplane. The circuit breaker timer protects against metal-oxide semiconductor field-effect transistor (MOSFET) overheating, enabling reliable protection against overstress.

The SMBus 3.1 interface, PMBus command structure, and on-board analog-to-digital converter (ADC) with selectable averaging and speed allow monitoring of board current, voltage, power, temperature, and fault status.

The LTC4286 has additional features to respond to input undervoltage (UV) and overvoltage (OV): interrupts the host when a fault occurs, notifies when output power is good, detects insertion of a board, and auto-reboot after a programmable delay following a host commanded turn off.

## TYPICAL APPLICATION

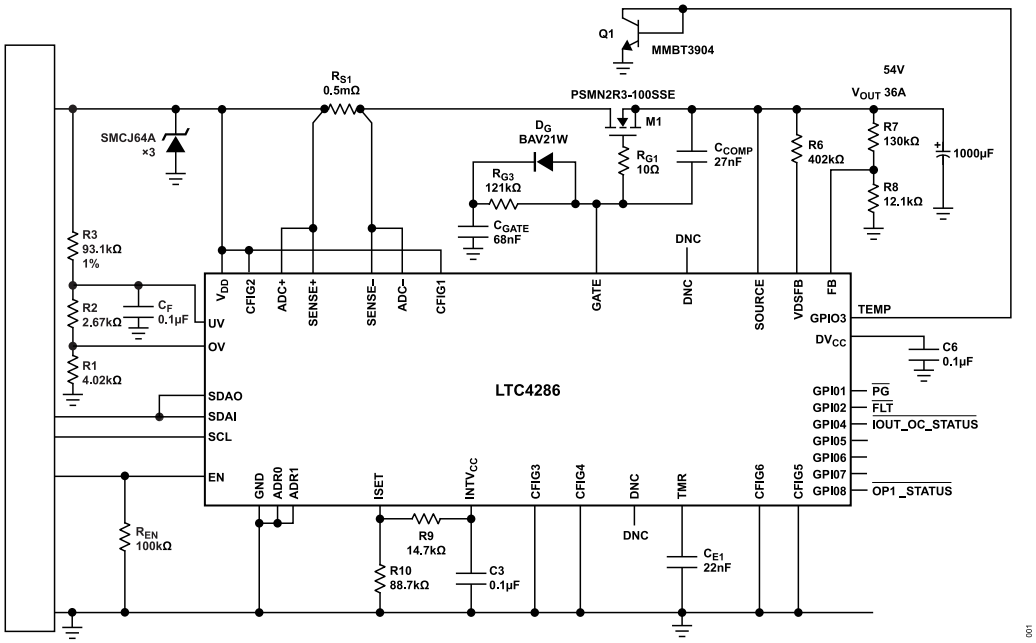


*Figure 1. 54 V, 1900 W Hot-Swap Controller*

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## REVISION HISTORY

**10/2023—Rev. 0 to Rev. A**

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**1/2023—Revision 0: Initial Version**

## ELECTRICAL CHARACTERISTICS

Specifications apply over the full operating temperature range, unless otherwise noted. All currents into pins are positive and all voltages are referenced to GND, unless otherwise specified.

***Table 1. Electrical Characteristics***

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| POWER SUPPLY | | | | | |
| Input Supply Range, $V_{DD}$ | | 8.5 | | 80 | V |
| Input Supply Current, $I_{DD}$ | No external resistor $V_{IN}$ to $INTV_{CC}$, no load on $DV_{CC}$ | | 12 | 18 | mA |
| | 5 kΩ pull-up on $INTV_{CC}$ from $V_{DD}$, 48 V, $T_A$ = 25°C, $V_{DD}$ = 48 V | | 1.8 | | mA |
| Input Supply Undervoltage Lockout, $V_{DD(UVLO)}$ | $V_{DD}$ rising | 5.75 | 6 | 6.35 | V |
| | $V_{DD}$ falling | 5.25 | 5.5 | 5.85 | V |
| Input Supply Undervoltage Lockout Hysteresis, $\Delta V_{DD(HYST)}$ | $T_A$ = 25°C, $V_{DD}$ = 48 V | | 0.5 | | V |
| $INTV_{CC}$ Output Voltage, $INTV_{CC}$ | $V_{DD}$ = 8.5 V and 80 V, $I_{LOAD}$ = 0 mA and –4 mA | 4.5 | 5 | 5.5 | V |
| $INTV_{CC}$ Undervoltage Lockout, $INTV_{CC(UVLO)}$ | $INTV_{CC}$ falling | 3.4 | 3.89 | 4.45 | V |
| | $INTV_{CC}$ rising | 3.6 | 4 | 4.5 | V |
| $INTV_{CC}$ Undervoltage Lockout Hysteresis, $\Delta INTV_{CC(UVLO)}$ | $T_A$ = 25°C, $V_{DD}$ = 48 V | | 115 | | mV |
| $DV_{CC}$ Output Voltage, $DV_{CC}$ | $V_{DD}$ = 8.5 V, 80 V, $I_{LOAD}$ = 0 mA | 4.5 | 5 | 5.5 | V |
| $DV_{CC}$ Undervoltage Lockout, $DV_{CC(UVLO)}$ | $DV_{CC}$ falling | 1.7 | 2 | 2.5 | V |
| | $DV_{CC}$ rising | 1.9 | 2.2 | 2.5 | V |
| $DV_{CC}$ Undervoltage Lockout Hysteresis, | $T_A$ = 25°C, $V_{DD}$ = 48 V | | 150 | | mV |
| GATE DRIVE | | | | | |
| External N-Channel Gate Drive at GATE ($V_{GATE}$ – $V_{SOURCE}$), $\Delta V_{GATE}$[1] | $V_{DD}$ = 8.5 V to 80 V, $I_{GATE}$ = 0 µA and –10 µA | 10 | 12 | 14 | V |
| GATE Pull-Up Current, $I_{GATE(UP)}$ | Gate drive on, $V_{GATE}$ = $V_{SOURCE}$ = 0 V | –35 | –53 | –70 | µA |
| GATE Pull-Down Current, $I_{GATE(DN)}$ | Gate drive on, $V_{GATE}$ = 58 V, $V_{SOURCE}$ = 48 V | 6 | 12 | 15 | mA |
| GATE Fast Pull-Down Current, $I_{GATE(FST)}$ | Fast turn off, $V_{GATE}$ = 58 V, $V_{OUT}$ = 48 V, $T_A$ = 25°C, $V_{DD}$ = 48 V | | 1 | | A |
| Gate-Source Voltage for FET-Bad and Power-Failed Faults, $V_{TH(GS)}$ | | 6 | 8 | 10 | V |
| ΔSENSE High to GATE Low Propagation Delay, $t_{PHL(SENSE)}$ | ILIM = 0000, $\Delta V_{SNS}$ = 0 to 100 mV step, $\Delta V_{GATE}$ = 6 V, $C_{GATE}$ = 10 nF, | | 0.5 | 1 | µs |
| GATE Off Propagation Delay: OV, $t_{PHL(GATE)OV}$ | OV = high, $\Delta V_{GATE}$ = 6 V gate open | | 1 | 2 | µs |
| GATE ON Propagation Delay:OV, $t_{PHL(GATE)OV}$ | OV = low | 0 | 5 | 10 | µs |
| GATE Off Propagation Delay: UV, $t_{PHL(GATE)UV}$ | UV = low, $\Delta V_{GATE}$ = 6 V gate open | 0.3 | 2 | 3 | µs |
| GATE Off Propagation Delay: EN, $t_{PHL(GATE)EN}$ | EN = low, $\Delta V_{GATE}$ = 6 V gate open | 15 | 40 | 70 | µs |
| $V_{DD}$ to Source Threshold Voltage for Power Bad Faults, $V_{DS(POWER\_BAD)}$ | $V_{DD}$ to source falling | 1.6 | 2.0 | 2.4 | V |
| FET Bad Fault Threshold (VDD-SOURCE) to start FETBAD timer, $V_{TH,FET-BAD}$ | $V_{DD}$ to source rising | 140 | 200 | 260 | mV |
| TIMING | | | | | |
| Power-Good Delay, $t_{DL(PG)}$ | | 172 | 181 | 190 | ms |
| Debounce Delay, Auto-Retry Delay Following Undervoltage Fault, $t_{DL(DB)}$ | | 86.1 | 90.6 | 95.2 | ms |
| FET BAD Delay, $t_{DL(FETBAD)}$ | | 0.138 | 0.145 | 0.152 | Sec |
| Auto-Retry Delay Following Overcurrent Fault, Input/ Output Fault, or FET Bad Fault, $t_{DL(RTRY)}$ | | 8.82 | 9.28 | 9.74 | Sec |
| Auto-Retry Counter Reset Delay, $t_{DL(RTCRST)}$ | VIN_UV_ FAULT_RETRY, VIN_OV_ FAULT_RETRY, OC_ FAULT_RETRY, OT_ FAULT_RETRY, OP_FAULT_RETRY = 001 to 110 | 88.2 | 92.8 | 97.4 | Sec |
| OP1 Fault Unit Delay, $t_{DL(OP1-UNIT)}$ | Delay = OP_TIMER(Value) × Unit Delay | 1.08 | 1.13 | 1.19 | ms |

## ELECTRICAL CHARACTERISTICS

*Table 1. Electrical Characteristics (Continued)*

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| CURRENT LIMIT | | | | | |
| Current-Limit Sense Voltage Threshold, ($V_{SENSE+}$ – $V_{SENSE–}$), $\Delta V_{SNS}$ | ILIM = 0001 | 5.67 | 6 | 6.33 | mV |
| | ILIM = 1111 | 18.55 | 20 | 21.45 | mV |
| Current-Limit Sense Voltage Linearity, $\Delta V_{SNS}$ | | | 0 | ±100 | µV |
| Foldback Factor, $\Delta V_{SNS}$ | 30% | 15 | 30 | 45 | % |
| Fast Pull-Down Threshold Multiplier, $V_{(TH)FPD}$ | $T_A$ = 25°C, $V_{DD}$ = 48 V | | 3 | | |
| SENSE+ Input Current, $I_{SENSE+(IN)}$ | SENSE– = SENSE+ = $V_{DD}$ | 0 | 120 | 250 | µA |
| SENSE– Input Current, $I_{SENSE–(IN)}$ | $V_{DD}$ – Source = 5 V | 4 | 5 | 6 | µA |
| OVERCURRENT TIMER | | | | | |
| TMR Fault Threshold, $V_{TMR(H)}$ | $V_{TMR}$ rising | 2.5 | 2.56 | 2.62 | V |
| TMR Low Threshold, $V_{TMR(L)}$ | $V_{TMR}$ falling | 0.18 | 0.2 | 0.22 | V |
| TMR Pull-Up Current, $I_{TMR(UP)}$ | $V_{TMR}$ = 0 V | –15 | –20 | –25 | µA |
| TMR Pull-Down Current, $I_{TMR(DN)}$ | $V_{TMR}$ = 2.56 V | 3 | 5 | 7 | µA |
| INPUT PINS | | | | | |
| UV/OV/FB Threshold Voltage, $V_{(TH)UV/OV/FB}$ | $V_{PIN}$ rising | 2.51 | 2.56 | 2.61 | V |
| OV Threshold Voltage, $V_{(TH)OV}$ | $V_{OV}$ falling | 2.3 | 2.5 | 2.6 | V |
| OV Hysteresis, $\Delta V_{(HYST)OV}$ | $T_A$ = 25°C, $V_{DD}$ = 48 V | | 55 | | mV |
| UV Threshold Voltage, $V_{(TH)UVF}$ | $V_{UV}$ falling | 2.15 | 2.2 | 2.25 | V |
| FB Threshold Voltage, $V_{(TH)FB}$ | $V_{FB}$ falling | 2.3 | 2.5 | 2.61 | V |
| FB Hysteresis, $\Delta V_{(HYST)FB}$ | $T_A$ = 25°C, $V_{DD}$ = 48 V | | 79 | | mV |
| UV Hysteresis, $\Delta V_{(HYST)UV}$ | $T_A$ = 25°C, $V_{DD}$ = 48 V | | 360 | | mV |
| UV Retry Threshold Voltage, $V_{(TH)UVR}$ | $V_{UVR}$ rising | 1 | 1.1 | 1.2 | V |
| UV Retry Threshold Voltage, $V_{(TH)UVR}$ | $V_{UVR}$ falling | 0.95 | 1.0 | 1.05 | V |
| UV Retry Threshold Hysteresis, $\Delta V_{(HYST)UVR}$ | $T_A$ = 25°C, $V_{DD}$ = 48 V | | 100 | | mV |
| ADR0, ADR1, Input High Threshold, $V_{ADR(H)}$ | | $INTV_{CC}$ – 0.8 | $INTV_{CC}$ – 0.5 | $INTV_{CC}$ – 0.2 | V |
| ADR0, ADR1, Input Low Threshold, $V_{ADR(L)}$ | | 0.2 | 0.5 | 0.8 | V |
| ADR0, ADR1, Input Current, $I_{ADR(IN)}$ | $V_{PIN}$ = 1 V, $V_{PIN}$ = $INTV_{CC}$ – 0.85 V | | | ±10 | µA |
| EN Threshold Voltage, $V_{EN(TH)}$ | $V_{EN}$ rising | 1.25 | 1.28 | 1.31 | V |
| | $V_{EN}$ falling | 1.225 | 1.26 | 1.295 | V |
| EN Hysteresis, $\Delta_{VEN(HYST)}$ | $T_A$ = 25°C, $V_{DD}$ = 48 V | | 20 | | mV |
| GPIO1-8 Pin Threshold Voltage, $V_{(TH)GPIO}$ | $V_{GPIO}$ rising | 1.25 | 1.28 | 1.31 | V |
| | $V_{GPIO}$ falling | 1.225 | 1.26 | 1.295 | V |
| GPIO1-8 Pin Hysteresis, $\Delta V_{(HYST)GPIO}$ | $T_A$ = 25°C, $V_{DD}$ = 48 V | | 20 | | mV |
| VDSFB Internal Resistor, $R_{VDSFB}$ | Gate on | 75 | 120 | 150 | kΩ |
| VDSFB Leakage Current, $I_{LEAK, VDSFB}$ | VDSFB = 0 V, $V_{DD}$ = 80 V, gate off | | 0 | ±1 | µA |
| SOURCE Input Current, $I_{SOURCE}$ | $V_{SOURCE}$ = 48 V, gate on | | | 300 | µA |
| | $V_{SOURCE}$ = 0 V, gate off | | | –200 | µA |
| | $V_{SOURCE}$ = 2 V, gate off | 0 | | 500 | µA |
| OV, UV, EN, FB Input Current, $I_{INPUT}$ | OV, UV, EN, FB = 2.5 V | | 0 | ±1 | µA |
| OUTPUT PINS | | | | | |
| GPIO1-8 Output Low Voltage, $V_{OL}$ | $I_{GPIO1\ to\ GPIO8}$ = 3 mA | | 0.2 | 0.5 | V |
| GPIO1-8 Leakage Current, $I_{LEAK,GPIO}$ | GPIO4, GPIO8 = 6 V, GPIO1, GPIO2, GPIO6 = 80 V, GPIO3, GPIO5, GPIO7 = $INTV_{CC}$ | | 0 | ±1 | µA |
| ADC | | | | | |
| Resolution (No Missing Codes)[2] | All channels | 12 | | | Bits |
| Full-Scale Voltage, $V_{FS}$ | $T_A$ = 25°C, $V_{DD}$ = 48 V | | | | |
| | (ADC+ – ADC–) | | 32 | | mV |
| | $V_{DS}$ | | 320 | | mV |

## ELECTRICAL CHARACTERISTICS

*Table 1. Electrical Characteristics (Continued)*

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| | $V_{DD}$/SOURCE, 25.6 V range | | 25 | | V |
| | $V_{DD}$/SOURCE, 100 V range | | 102.4 | | V |
| LSB Step Voltage, LSB | (ADC+ − ADC–), $T_A$ = 25°C, $V_{DD}$ = 48 V | | 7.8 | | µV |
| | $V_{DS}$ | | 78 | | µV |
| | $V_{DD}$/SOURCE, 25 V range | | 6.25 | | mV |
| | $V_{DD}$/SOURCE, 100 V range | | 25 | | mV |
| Offset Error, $V_{OS}$ | ADC+ – ADC | | | ±20 | LSB |
| | $V_{DD}$/SOURCE, $T_A$ = 25°C, $V_{DD}$ = 48 V | | | ±10 | LSB |
| | $V_{DS}$ | –10 | | 50 | LSB |
| Integral Nonlinearity, INL | (ADC+ − ADC–), $V_{DD}$/SOURCE, $V_{DS}$, $T_A$ = 25°C, $V_{DD}$ = 48 V | | ±1 | | LSB |
| Full-Scale Error, FSE | (ADC+ − ADC–), $V_{DD}$/SOURCE | | | ±1 | % |
| | $V_{DS}$ | −3 | | +1 | % |
| Refresh Rate in Continuous Mode, Internal Oscillator, $f_{CONV}$ | (ADC+ − ADC–), $V_{DD}$/SOURCE, power | 3.36 | 3.53 | 3.71 | kHz |
| | $V_{DS}$ | 1.68 | 1.77 | 1.86 | kHz |
| Individual Channel Conversion Time, Internal Oscillator, $t_{CONV}$ | (ADC+ − ADC–), $V_{DS}$ | 269 | 283 | 310 | µs |
| | $V_{DD}$/SOURCE | 269 | 283 | 310 | µs |
| ADC+ Input Current, $I_{ADC+}$ | $V_{(ADC+)}$ = $V_{DD}$ = 48 V, $V_{(ADC–)}$ = $V_{DD}$ – 21.3 mV | | 73 | 132 | µA |
| ADC– Input Current, $I_{ADC–}$ | $V_{(ADC+)}$ = $V_{DD}$ = 48V, $V_{(ADC–)}$ = $V_{DD}$ – 21.3 mV | | 0 | ±1 | µA |
| TEMPERATURE MEASUREMENT | | | | | |
| Resolution (No Missing Codes)[2] | | | 10 | | Bits |
| Refresh Rate in Continuous Mode, $f_{TCONV}$ | | | 3.45 | | Hz |
| Full-Scale Temperature Range, $R_{TFS}$ | $T_A$ = 25°C, $V_{DD}$ = 48 V | –273 | | 751 | °C |
| Temperature Measurement Range, $R_{TOP}$ | $T_A$ = 25°C, $V_{DD}$ = 48 V | –55 | | 175 | °C |
| Remote Temperature Error, η = 1.004, $T_{RMT}$ | –40°C to 125°C[3], $T_A$ = 25°C, $V_{DD}$ = 48 V | | ±1 | ±10 | °C |
| Temperature LSB Step, $LSB_{TEMP}$ | $T_A$ = 25°C, $V_{DD}$ = 48 V | | 1 | | °C |
| TEMP Current, $I_{TEMP}$ | Low level, $T_A$ = 25°C, $V_{DD}$ = 48 V | | 10 | | µA |
| | Midlevel, $T_A$ = 25°C, $V_{DD}$ = 48 V | | 80 | | µA |
| | High level, $T_A$ = 25°C, $V_{DD}$ = 48 V | | 150 | | µA |
| SMBus INTERFACE[4] | | | | | |
| SDAO Output Low Voltage, $V_{SDAO(OL)}$ | ISDAO = 20 mA | | | 0.5 | V |
| SDAO Input Current, $I_{SDAO}$ | SDAO = 5 V | | 0 | ±1 | µA |
| SDAI, SCL Input Threshold, $V_{SDAI,SCL(TH)}$ | | 0.9 | 1.1 | 1.35 | V |
| SDAI, SCL Input Current, $I_{SDAI,SCL}$ | SDAI, SCL= 5 V | | 0 | ±1 | µA |
| SMBus INTERFACE TIMING[2,4] | | | | | |
| SCL Clock Frequency, $f_{SCL}$ | $T_A$ = 25°C, $V_{DD}$ = 48 V | 10 | | 1000 | kHz |
| SCL Low Period, $t_{LOW}$ | $T_A$ = 25°C, $V_{DD}$ = 48 V | 0.40 | | | µs |
| SCL High Period, $t_{HIGH}$ | $T_A$ = 25°C, $V_{DD}$ = 48 V | 0.20 | | | µs |
| Data Setup Time, $t_{SU,DAT}$ | SDAI setup from SCL ↑ for data, $T_A$ = 25°C, $V_{DD}$ = 48 V | 20 | | | ns |
| Data Hold Time, $t_{HD,DAT}$ | SDAI hold from SCL ↓ for data, $T_A$ = 25°C, $V_{DD}$ = 48 V | 0 | | | ns |
| Hold Time Start Bit, $t_{HD,STA}$ | SCL high after SDAI ↓, $T_A$ = 25°C, $V_{DD}$ = 48 V | 160 | | | ns |
| Setup Time for Repeated Start, $t_{SU,STA}$ | SCL high setup to SDAI ↓, $T_A$ = 25°C, $V_{DD}$ = 48 V | 160 | | | ns |
| Setup Time for Stop Bit, $t_{SU,STO}$ | SCL high setup to SDAI ↑, $T_A$ = 25°C, $V_{DD}$ = 48 V | 160 | | | ns |
| SDAO Delay, $t_{DEL,SDAO}$ | SDAO ↓ delay from SCL ↓, SEL_1M = 0, $T_A$ = 25°C, $V_{DD}$ = 48 V | 100 | 175 | 405 | ns |
| | SDAO ↓ delay from SCL ↓, SEL_1M = 1, $T_A$ = 25°C, $V_{DD}$ = 48 V | 75 | 125 | 220 | ns |
| SCL or SDAI Pulse Spike Rejection, $t_{PW}$[2] | $T_A$ = 25°C, $V_{DD}$ = 48 V | 55 | 75 | 110 | ns |
| PMBus Stuck Bus Timeout, $T_{D(STUCK)}$ | $T_A$ = 25°C, $V_{DD}$ = 48 V | 25 | 30 | 35 | ms |

## ELECTRICAL CHARACTERISTICS

*Table 1. Electrical Characteristics (Continued)*

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| SCL, SDA Input Capacitance, $C_X$ | SDAI tied to SDAO, $T_A$ = 25°C, $V_{DD}$ = 48 V | | 5 | 10 | pF |

1 An internal clamp limits the GATE pin to a minimum of 10 V above SOURCE. Driving this pin to voltages beyond the clamp can damage the device.

2 Guaranteed by design and characterization.

3 Remote diode temperature, not LTC4286 temperature. Guaranteed by design and test correlation.

4 The LTC4286 is fully compliant with SMBus 3.1 and operation up to 1 Mbps. In general, the chip can be used in $I^2C$ bus systems using standard-mode, fast-mode, or fast-mode plus as long as PMBus command protocols are followed. A $V_{IH}/V_{IL}$ incompatibility between SMBus 3.1 and $I^2C$ can lead to a DC level violation for $I^2C$ buses running at 3.5 V or higher.

## ABSOLUTE MAXIMUM RATINGS

All currents into pins are positive and all voltages are referenced to GND, unless otherwise specified.

*Table 2. Absolute Maximum Ratings*

| Parameter | Rating |
|---|---|
| Supply Voltages | |
| $V_{DD}$ | −0.3 V to +100 V |
| $INTV_{CC}$, $DV_{CC}$ | −0.3 V to +5.5 V |
| Input Voltages | |
| SDAI, SCL | −0.3 V to +6 V |
| CFIG4 | −0.3 V to +1 V |
| OV, UV, FB, EN | −0.3 V to +100 V |
| VDSFB | −0.3 V to $V_{DD}$ + 0.3 V |
| TMR, ADR0, ADR1, CFIG3 | −0.3 V to $INTV_{CC}$ + 0.3 V |
| ADC+, SENSE+ | $V_{DD}$ − +4.5 V to $V_{DD}$ + 0.3 V |
| ADC−, SENSE− | $V_{DD}$ − +4.5 V to $V_{DD}$ + 0.3 V |
| CFIG1, CFIG2 | $V_{DD}$ − +4.5 V to $V_{DD}$ + 0.3 V |
| SOURCE | −0.3 V to +100 V |
| GATE − SOURCE[1] | −0.3 V to +10 V |
| Output Voltages | |
| ISET, CFIG5, CFIG6 | −0.3 V to $DV_{CC}$ + 0.3 V |
| GPIO1, GPIO2, GPIO6 | −0.3 V to 100 V |
| GPIO3, GPIO5, GPIO7 | −0.3 V to $INTV_{CC}$ + 0.3 V |
| GATE | −0.3 V to +100 V |
| SDAO, GPIO4, GPIO8 | −0.3 V to +6 V |
| Output Currents | |
| $INTV_{CC}$, $DV_{CC}$ | −5 mA |
| Temperature | |
| Operating Range | −40°C to +125°C |
| Storage Range | −65°C to +150°C |

[1] An internal clamp limits the GATE pin to a minimum of 10 V above SOURCE. Driving this pin to voltages beyond the clamp may damage the device.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device**. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

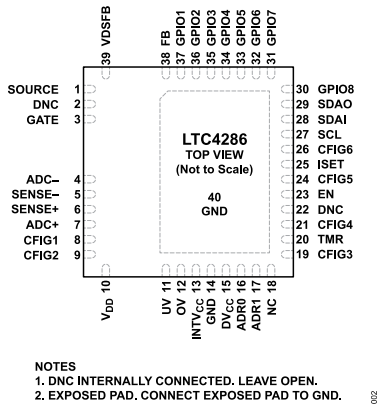


*Figure 2. Pin Configuration*

*Table 3. Pin Function Descriptions*

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | SOURCE | N-channel MOSFET Source and ADC Input. Connect this pin to the source of the external N-channel MOSFET. This pin provides a return for the GATE pull-down circuit, is used as an input to the 200 mV and 2 V $V_{DS}$ comparators that are used for FET-BAD faults and Power_Good, respectively. The SOURCE pin also serves as an ADC input to monitor the output voltage. |
| 2, 22 | DNC | Do not connect. Leave open. |
| 3 | GATE | Gate Drive Output for External N-channel MOSFET. Internal 53 µA current source charges the gate of the MOSFET. No compensation capacitors are required on the GATE pin, but an RC network from this pin to ground can be used to set the turn-on output voltage slew rate. During turn-off, there is a 12 mA pull-down current to SOURCE. During a short-circuit or undervoltage lockout ($V_{DD}$, $INTV_{CC}$), a 1 A pull-down between GATE and SOURCE is activated. |
| 4 | ADC− | Negative Kelvin ADC Current Sense Input. Connect this pin to the output side of the current sense resistor or a resistive averaging network when using multiple sense resistors. |
| 5 | SENSE− | Negative Kelvin Current Sense Input. Connect this pin to the MOSFET side of the current sense resistor. The current-limit circuit controls the GATE pin to limit the sense voltage between the SENSE+ and SENSE− pins to the limit value selected by the ISET pin. |
| 6 | SENSE+ | Positive Kelvin Current Sense Input. Connect this pin to the $V_{DD}$ side of the current sense resistor. |
| 7 | ADC+ | Positive Kelvin ADC Current Sense Input. Connect this pin to the input side of the current sense resistor or a resistive averaging network when using multiple sense resistors. Must be connected to the same trace as $V_{DD}$ or a resistive averaging network, which adds up to 1 Ω to $V_{DD}$. |
| 8 | CFIG1 | Configuration Input. Tie to $V_{DD}$. |
| 9 | CFIG2 | Configuration Input. Tie to $V_{DD}$. |
| 10 | $V_{DD}$ | Supply Voltage Input. This pin has an undervoltage lockout threshold of 6 V. $V_{DD}$ is an input for the FET-BAD comparator with a 200 mV threshold. It is also an input for the power bad comparator with a 2 V threshold. The ADC can be configured to measure the voltage at this pin. |
| 11 | UV | Undervoltage Comparator Input. Connect this pin to an external resistive-divider from $V_{DD}$ to GND. If the UV pin falls below 2.2 V, an undervoltage occurs, and the MOSFET turns off. If the UV pin rises above 2.56 V, the MOSFET turns on after a debounce delay of 90.6 ms. Pulling this pin below 1 V adds one retry to the retry counter for an OC, FET_BAD, OT, or OP fault, which is linked to the FAULT# GPIO output in MFR_FLT_CONFIG if that fault has zero remaining retries. If overcurrent auto-retry is required, then tie this pin to the GPIO2 pin, which is configured as a FAULT# output reporting OC and FET_BAD faults by default. Tie to $INTV_{CC}$ if unused or connect to a GPIO pin with a 4.7 kΩ pull-up to $INTV_{CC}$ if only the auto-retry function is used. |
| 12 | OV | Overvoltage Comparator Input. Connect OV to an external resistive voltage-divider from $V_{DD}$ to GND. An overvoltage fault occurs if this pin rises above the 2.56 V threshold. When the OV pin voltage falls back below the 2.5 V falling threshold, the GATE pin turns on again immediately. Tie to GND if unused. |
| 13 | $INTV_{CC}$ | Internal Supply Decoupling Output. Connect a capacitor no smaller than 0.1 µF from this pin to the ground. Up to 5 mA can be drawn from this pin to power 5 V application circuitry. This pin is current-limited and drops to GND to reduce heating in an overcurrent condition. Overloading this pin can disrupt internal operation. To reduce heating, |

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

*Table 3. Pin Function Descriptions (Continued)*

| Pin No. | Mnemonic | Description |
|---|---|---|
| | | this pin can act as a shunt regulator by connecting a resistor to $V_{DD}$ or another supply such that 10 mA flows to $INTV_{CC}$. |
| 14 | GND | Device Ground. |
| 15 | $DV_{CC}$ | 5 V Internal Logic Supply Output. This is an output of the internal linear regulator with an UVLO threshold of DVCC (UVLO). The voltage at this pin powers up the logic control circuitry and SMBus interface. Bypass this pin with a 0.1 µF capacitor. |
| 16, 17 | ADR0, ADR1 | Serial Bus Address Inputs. Tying these pins to ground (L), open (NC) or $INTV_{CC}$ (H) configures one of nine possible addresses. See Table 9. |
| 18 | NC | Not internally connected. |
| 19 | CFIG3 | Configuration Input. Tie to GND. |
| 20 | TMR | Current-Limit Timer. Connect a capacitor between this pin and ground to set a 128 ms/µF duration for current limit before the MOSFET is turned off. If configured to auto-retry or if the UV pin is toggled low, the MOSFET turns on again following a cool-down time of 9.28 s. |
| 21 | CFIG4 | Configuration Input. Tie to GND. |
| 23 | EN | Active High Enable Input. EN is typically used to indicate that a board is present. The external MOSFET can only be turned on when EN is active and the ON bit in the OPERATION register is set. See Table 4 for the ON bit defaults at power-up. Any transition on this pin sets the EN_CHANGED bit in MFR_SPECIFIC_STATUS. |
| 24 | CFIG5 | Configuration Input. Tie to GND. |
| 25 | ISET | Current-Limit Adjustment Input. The ISET voltage is compared with seven threshold voltages generated by a resistive voltage-divider from $INTV_{CC}$. The result sets the current-limit voltage to be one of eight discrete values from 6 mV to 20 mV in 2 mV increments. When ISET is connected to ground, the current-limit threshold is set to 6 mV. When ISET is connected to $INTV_{CC}$, current-limit threshold is set to 20 mV (see Table 5). |
| 26 | CFIG6 | Initial ON Configuration Input. Tie to GND to turn on automatically, tie to 1.6 V with a resistive divider to remain off awaiting further instructions. For more details, see Table 4. |
| 27 | SCL | SMBus-compatible Clock Input, high impedance. |
| 28 | SDAI | Serial Bus Data Input. A high impedance input for shifting in address, command, or data bits. Normally tied to SDAO to form the SDA line. |
| 29 | SDAO | Serial Bus Data Output. Open-drain output for sending data back to the controller or acknowledging a write operation. Normally tied to SDAI to form the SDA line. An external pull-up resistor or current source is required. |
| 30 | GPIO8 | OP1_STATUS# Indicator Output. This pin is pulled low when the ADCs measure a power level above the OP1 threshold. Tie to GND if unused. |
| 31 | GPIO7 | Comparator Output. This pin is the output of the comparator on the GPIO6 pin. Tie to GND if unused. |
| 32 | GPIO6 | Comparator Input. This pin has a 1.28 V threshold. The output of the comparator is available on GPIO7. Tie to GND if unused. |
| 33 | GPIO5 | This pin has a reserved function by default. Leave it open unless changing its configuration register. |
| 34 | GPIO4 | IOUT_OC_STATUS# Indicator Output. When the LTC4286 is in current limit, this open-drain output is pulled low to indicate an overcurrent condition. Tie to GND if unused. |
| 35 | GPIO3 | Temperature Sensor Input. Connect to an MMBT3904 transistor for use as a remote temperature sensor. Tie to GND if unused. |
| 36 | GPIO2 | FAULT# Output. This pin pulls low when an overcurrent or FET-BAD fault occurs. This pin can be tied to the UV pin to clear faults and auto-retry after a fault occurs. Tie to GND if unused. |
| 37 | GPIO1 | Power-Good# Indicator Output. This open drain pull-down pulls low when power is good, as determined by the FB pin and GATE pin voltages. Tie to GND if unused. |
| 30 to 37 | GPIO1 to GPIO8 | General-purpose I/O with open-drain output drivers. Several digital I/O functions are available for these pins. Those functions can be assigned by configuration to any of the eight pins. With few exceptions, the pins behave identically. GPIO1, GPIO2, and GPIO6 can be externally pulled as high as $V_{DD}$. The others must not be pulled any higher than $DV_{CC}$. The external temperature sensor function is available on GPIO3 only. Individual GPIO pin descriptions further refer to the hardware default configuration. By default, all alerts are disabled, and no GPIO pins are assigned to ALERT#, which can be changed after power-up by writing configuration registers. |
| 38 | FB | Power-Good Input. Connect this pin to an external resistive divider from SOURCE to GND. When the voltage at this pin drops below 2.56 V, power is not considered good. The power bad condition can result in a GPIO Power Good# pin pulling low or going high impedance depending on the GPIO pin configuration. Also a power bad fault is logged in this condition if a GATE pin is high. Tie to $INTV_{CC}$ if unused. |

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

*Table 3. Pin Function Descriptions (Continued)*

| Pin No. | Mnemonic | Description |
|---|---|---|
| 39 | VDSFB | VDS Foldback Sense Input. This pin is used to monitor the drain to source voltage of the external MOSFETs, which is used to set the foldback current limit. VDSFB is tied to SOURCE for 12 V applications, and an additional 10 kΩ/V is added for higher operating voltages, to set the proper gain of the foldback circuit. |
| 40 | EPAD (GND) | Exposed Pad. Connect exposed pad to GND. |

## TYPICAL PERFORMANCE CHARACTERISTICS

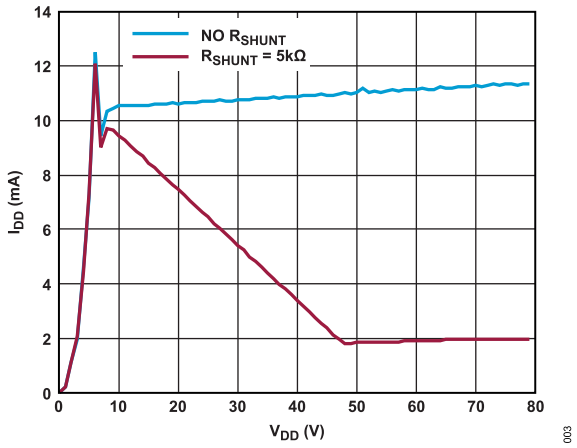


*Figure 3. $I_{DD}$ vs. $V_{DD}$*

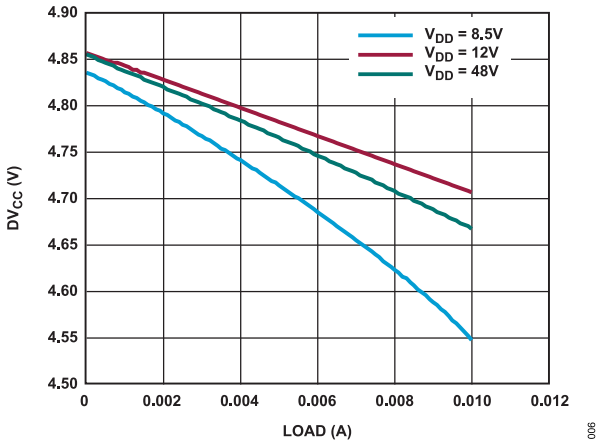


*Figure 6. $DV_{CC}$ vs. Load at $V_{DD}$ = 8.5 V, 12 V, and 48 V*

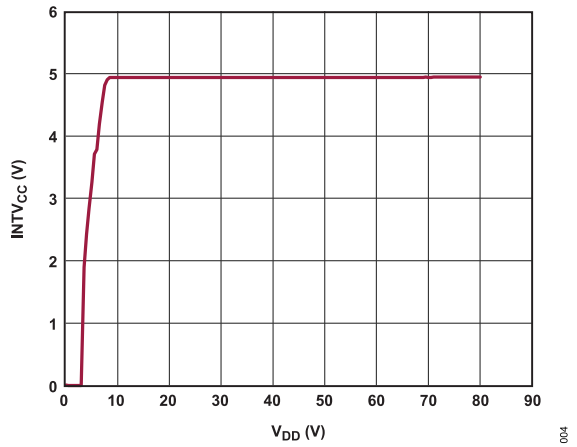


*Figure 4. $INTV_{CC}$ vs. $V_{DD}$*

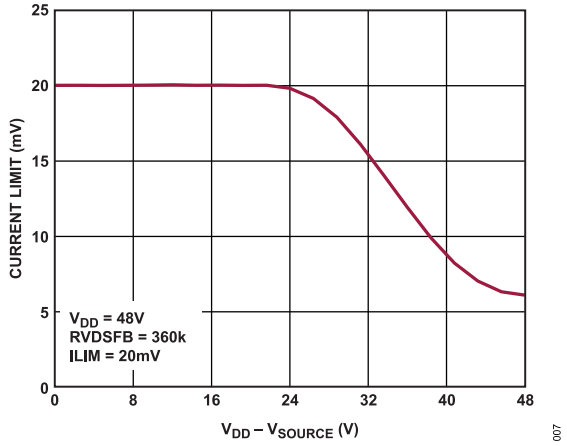


*Figure 7. Current-Limit Foldback Profiles*

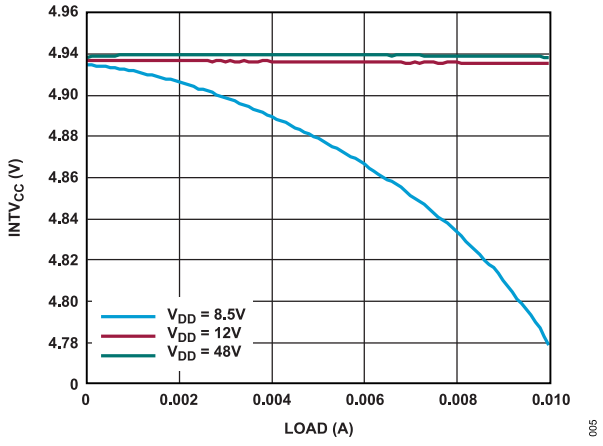


*Figure 5. $INTV_{CC}$ vs. Load at $V_{DD}$ = 8.5 V, 12 V, and 48 V*

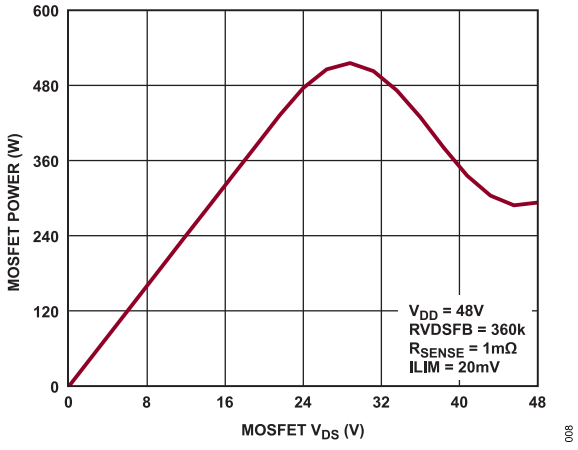


*Figure 8. MOSFET Power vs. $V_{DS}$*

## TYPICAL PERFORMANCE CHARACTERISTICS

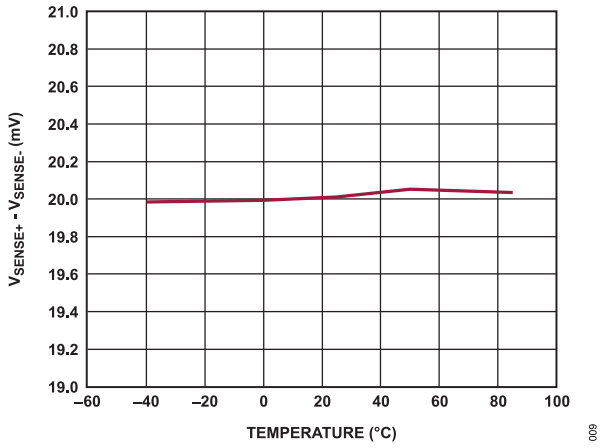


*Figure 9. Current-Limit Threshold vs. Temperature*

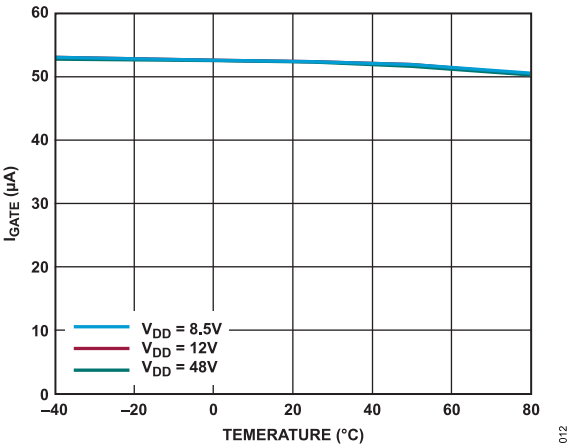


*Figure 12. IGATE (Up) vs. Temperature*

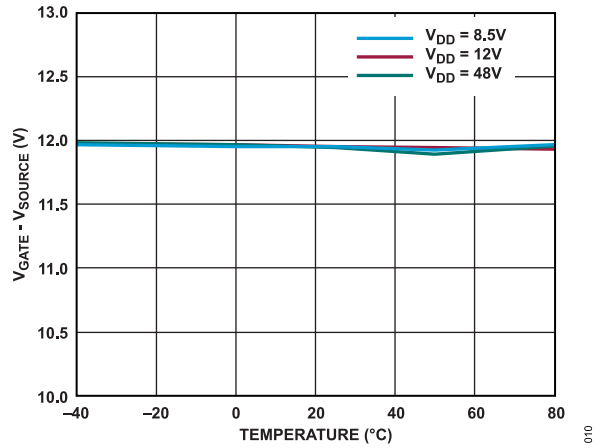


*Figure 10. $V_{GATE}$ – $V_{SOURCE}$ vs. Temperature at $V_{DD}$ = 8.5 V, 12 V, and 48 V*

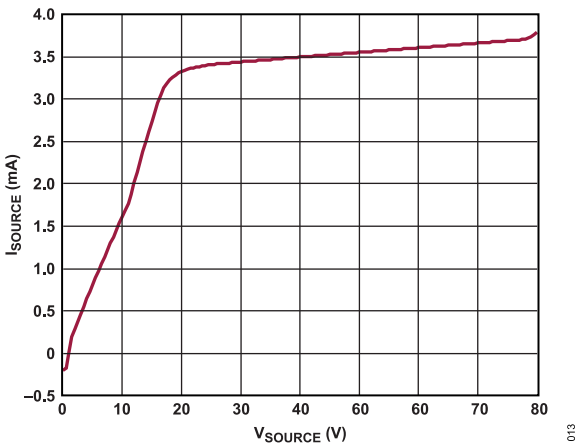


*Figure 13. $I_{SOURCE}$ vs. $V_{SOURCE}$*

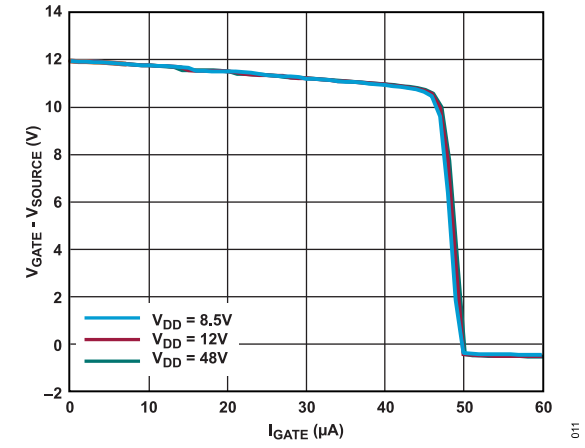


*Figure 11. $V_{GATE}$ – $V_{SOURCE}$ vs. IGATE (Leak) at $V_{DD}$ = 8.5 V, 12 V, and 48 V*

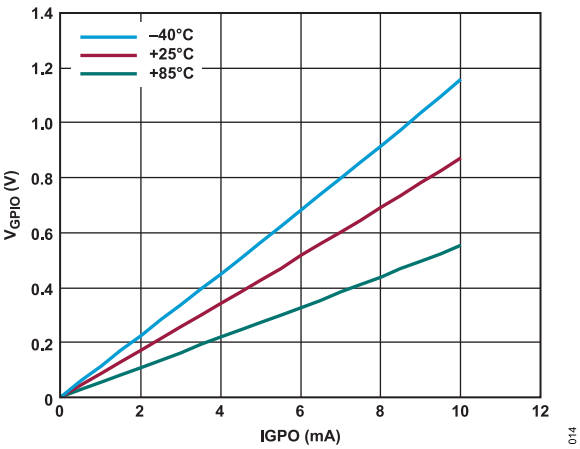


*Figure 14. $V_{OL}$ GPIO1, GPIO2, GPIO6 vs. IGPO*

## TYPICAL PERFORMANCE CHARACTERISTICS

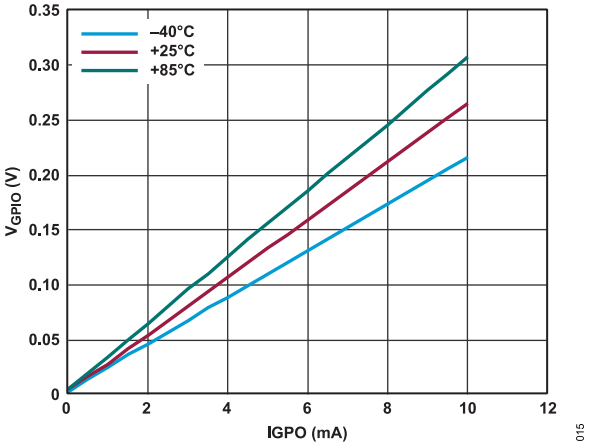


*Figure 15. $V_{OL}$ GPIO3, GPIO5, GPIO7 vs. IGPO*

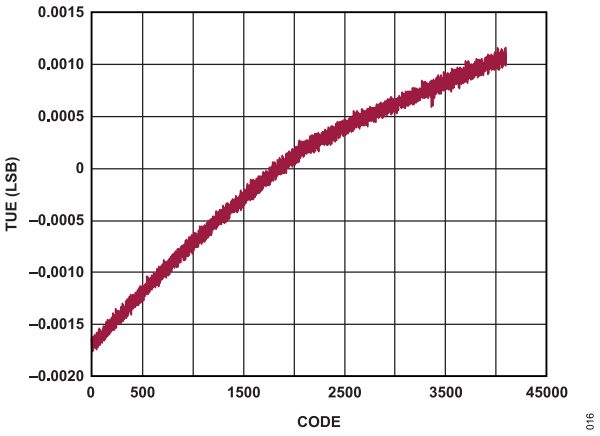


*Figure 16. ADC TUE vs. Code (64x Average)*

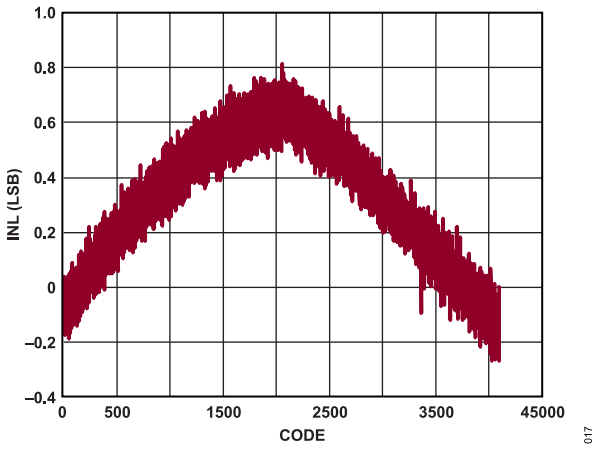


*Figure 17. ADC INL vs. Code (64x Average)*

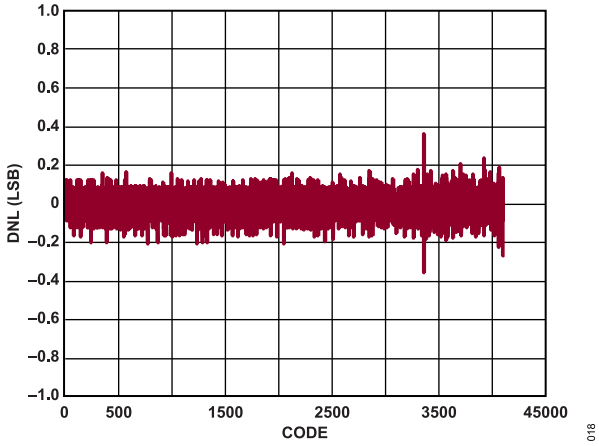


*Figure 18. ADC DNL vs. Code (64x Average)*

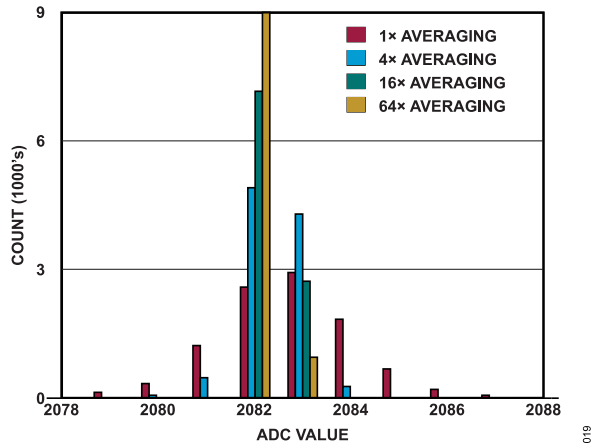


*Figure 19. 12-Bit Current ADC Noise Histogram (1x, 4x, 16x, and 64x Average)*

## THEORY OF OPERATION

The LTC4286 is designed to turn a board's supply voltage on and off in a controlled manner, allowing the board to be safely inserted or removed from a live backplane. During normal operation, the charge pump and gate driver turn on an external N-channel MOSFET gate to pass power to the load. The gate driver uses a charge pump that derives its power from the $V_{DD}$ pin. Also, included in the gate driver is an internal 14 V GATE to SOURCE clamp to protect the oxide of the external MOSFET.

In normal operation, the LTC4286 turns on the external N-channel MOSFET after a startup debounce delay, passing power to the load. A precise current limit value can be set from 6 mV to 20 mV in 2 mV steps using ISET voltage or bits in the MFR_CONFIG1 register. During startup, the voltage between SENSE+ and SENSE− is controlled to be no higher than the current limit threshold with foldback (α). The startup current may be set to even lower values with an external gate RC network.

An overcurrent fault at the output may result in excessive MOSFET power dissipation during active current limiting (ACL). To limit this power, the ACL amplifier regulates the voltage between the SENSE+ and SENSE− pins by reducing the gate-to-source voltage in an active control loop when the sense voltage exceeds the current-limit value. When the MOSFET drain to source voltage is high, power dissipation is further reduced by folding back the current limit to 30% of nominal. In the event of a catastrophic output short, fast current limit comparators immediately pull the GATE pin down with 1 A when the sensed current is three times the nominal current-limit.

To prevent MOSFET overheating, the current-limit timeout is set by a capacitor on the TMR pin. The TMR pin is configured to drive a single capacitor and ramp up with 20 µA when active current limiting is engaged. If the TMR pin reaches its 2.56 V threshold, the LTC4286 turns off GATE and the IOUT_OC_FAULT bit is set, which causes the FAULT# pin to pull low. Then the TMR pin ramps down using a 5 µA current source until the voltage drops below 0.2 V. If overcurrent auto-retry is enabled by tying the GPIO2 (configured as FAULT#) pin to the UV pin, the LTC4286 turns on again at the end of the 9.28 s cool-down timer.

The output voltage is monitored using the SOURCE pin and the power good (PG) comparator to determine if the power is available for the load. The power good condition is signaled by the GPIO1 (configured as Power-Good#) pin using an open-drain pull-down transistor.

The LTC4286 includes three ADCs and all operate at 12-bit resolution. One data converter continuously monitors the ADC+ to ADC− voltage, sampling every 1 µs and producing a 12-bit result of the average sense voltage every 283 µs. The second data converter is synchronized to the first and measures the SOURCE voltage during the same time period. Every time the first two ADCs finish taking a measurement, the sense voltage is multiplied by the measurement of the SOURCE pin to provide a power measurement. The third data converter measures temperature on an external or internal diode with 1°C resolution. The minimum and maximum SOURCE, ADC+ to ADC−, POWER, and TEMP measurements are stored, and optional alerts may be generated if a measurement is above or below user configurable 12-bit thresholds.

A PMBus interface is provided to read the A/D registers. It also allows the host to poll the device and determine if faults have occurred. If any GPIO pin is configured as an ALERT# interrupt, the host is enabled to respond to faults in real time. The PMBus device target address is decoded using the ADR0 and ADR1 pins. These inputs have three states each that decode into a total of nine device addresses.

## APPLICATIONS INFORMATION

A typical LTC4286 application is in a high availability system in which a positive voltage supply is distributed to power individual boards. PMBus telemetry includes voltages, currents, and status information including faults to be read by the host. The LTC4286 stores minimum and maximum ADC measurements, calculates power, and can be configured to generate alerts based on measurement results, avoiding the need for the system to poll the device on a regular basis. A basic LTC4286 application circuit is shown in Figure 1. The following sections cover turn-on, turn-off, and various faults that the LTC4286 detects and acts upon.

### OVERVIEW

The output is controlled by using a N-channel MOSFET, M1, placed in the power path. The resistor RS1 provides the current measurement. The resistive dividers R1, R2, and R3 define undervoltage and overvoltage levels. The UV and OV thresholds can be set using a three resistor dividers. Choose a divider current of at least 200 µA. R1 < 2.56 V/200 µA = 12.8 kΩ, then calculate:

$$R2 = \frac{V_{OV(OFF)}}{V_{UV(ON)}} \times R1 \times \frac{UV_{TH(RISING)}}{OV_{TH(FALLING)}} - R1 \quad (1)$$

$$R3 = \frac{V_{UV(ON)} \times (R1 + R2)}{UV_{TH(RISING)}} - R1 - R2 \quad (2)$$

The resistor RG1 prevents high frequency self-oscillations in the MOSFET. R7 and R8 set the power-good threshold, and R6 scales current-limit foldback to the intended operating voltage. The resistive divider, R9 and R10, sets the value of the current limit. For more details, see Table 5.

### TURN-ON SEQUENCE

Several conditions must be present before the external MOSFETs turn on. First, the external supply, $V_{DD}$, must exceed its 6.0 V undervoltage lockout level. Next, the internally generated supplies, $INTV_{CC}$ and $DV_{CC}$, must cross their 4 V and 2.2 V undervoltage thresholds, respectively. This generates an internal power-on reset signal. After a power-on reset, the UV and OV pins verify that input power is within the acceptable range and the EN pin must be made active to indicate that the board is seated, or the LTC4286 is commanded to turn on. The state of the UV and EN comparators must be stable for at least 90.6 ms to qualify for turn on. When these conditions are satisfied, turn on is initiated. The MOSFET is then turned on by charging up the GATE pin with a 53 µA current source. When the GATE pin voltage reaches the MOSFET threshold voltage, the MOSFET begins to turn on and the SOURCE voltage then follows the GATE voltage as it increases. The capacitor $C_{GATE}$ limits the dv/dt on the GATE voltage, controlling the inrush current. The inrush current is:

$$I_{INRUSH} = I_{GATE(UP)} \times \frac{C_{LOAD}}{C_{GATE}} \quad (3)$$

Once the MOSFET drain to source voltage is lower than its 2 V threshold, the GATE pin reaches higher than its 8 V threshold, and the FB pin exceeds its 2.56 V threshold, a GPIO pin configured as a power-good output releases high to indicate that power is good and the load can be activated. The CFIG6 pin is used to select if the LTC4286 starts up automatically after power up or waits for a PMBus host controller to command it to turn on. If the CFIG6 pin is grounded, it turns on, if it is set to 1.6 V by a resistive divider, it remains off and wait for further instructions. See Table 4.

*Table 4. Using the CFIG6 Pin to Configure the Default On/Off State*

| CFIG6 at Power-Up | ON Bit |
|---|---|
| <1 V | On |
| >1 V, <2.56 V | Off |

At the minimum input supply voltage of 8.5 V, the minimum GATE-to-SOURCE driver voltage is 10 V. The GATE-to-SOURCE voltage is clamped below 14 V to protect the gates of 20 V N-channel MOSFETs. A curve of GATE-to-SOURCE drive ($\Delta V_{GATE}$) vs. $V_{DD}$ is shown in the Typical Performance Characteristics section.

### TURN-OFF SEQUENCE

A normal turn-off sequence is initiated by card withdrawal when the backplane connector short pin connected to EN opens, causing the EN pin to change state. Additionally, several fault conditions turn off the GATE pin. These include an input overvoltage, input undervoltage, overcurrent, or FET-BAD fault. The MOSFET is turned off with 1 mA of current pulling the GATE pin to ground combined with 11 mA from GATE-to-SOURCE, for a total of 12 mA. With the MOSFET turned off, the SOURCE and FB voltages drop as the load capacitance discharges. When the FB voltage crosses below its threshold, a GPIO pin configures as a power-good output pulls low to indicate that the output power is no longer good. If the $V_{DD}$ pin falls to less than 5.5 V or $INTV_{CC}$ drops to less than the undervoltage lockout falling threshold of 3.89 V, a fast shut down of the MOSFET is initiated. The GATE pin is then pulled down with 1 A of current to the SOURCE pin.

#### Overcurrent Fault Condition

The current limit is set by the value of the ILIM bits in the MFR_CONFIG1 register and the value of the current-sense resistor, RS1. In the event of an overcurrent, the power-dissipation in the MOSFET is limited by the foldback profile shown in Figure 7 and Figure 8. Calculate the value of the external resistor, R6:

$$R6 = 10\ \text{k}\Omega \times (V_{IN} - 12\ \text{V}) \quad (4)$$

Examples include the following:

- $V_{IN}$ = 12 V, $R_{VDSFB}$ = 0 Ω
- $V_{IN}$ = 48 V, $R_{VDSFB}$ = 365 kΩ

### MOSFET SOA-TIMER CAPACITOR

MOSFET manufacturers specify the safe limits on operating voltage, current, and time as a set of curves referred to as the safe operating area (SOA). The proper timer capacitance must be set to allow the worst-case operating condition to stay within the SOA

## APPLICATIONS INFORMATION

limits. The worst-case operating condition can be completely charging a large bypass capacitor at the output during start up or riding through a large input step. The capacitor on the TIMER pin must be calculated to ensure that the MOSFET stays within the SOA during normal and fault conditions.

Note that the timer is independent of the current limit. If the current limit is changed, it may be necessary to change the value of the TIMER pin capacitor.

### Setting the Current Limit

The current limit is set with a resistive divider on the ISET pin. The ISET pin provides a 2 mV resolution. These options are shown in Table 5. ISET is only read at power-up or reboots. Changing ISET while operating does not change the current limit. Writing to ILIM while operating changes the current-limit.

*Table 5. Configuring Current Limit with the ISET Pin*

| | | | ISET Thresholds Compared with | | | | |
|---|---|---|---|---|---|---|---|
| $\Delta V_{SNS(TH)}$ (mV) | ILIM | $V_{ISET}$ (V) | Lower (V) | Upper (V) | $R_{TOP}$ (kΩ) | $R_{BOTTOM}$ (kΩ) | $R_{BOTTOM}/(R_{TOP} + R_{BOTTOM})$ |
| 6 | 0001 | 0 | | 0.357 | Open | Short | 0.000 |
| 8 | 0011 | 0.714 | 0.357 | 1.071 | 88.7 | 14.7 | 0.143 |
| 10 | 0101 | 1.429 | 1.071 | 1.786 | 73.2 | 29.4 | 0.286 |
| 12 | 0111 | 2.143 | 1.786 | 2.5 | 59.0 | 44.2 | 0.429 |
| 14 | 1001 | 2.857 | 2.5 | 3.214 | 44.2 | 59.0 | 0.571 |
| 16 | 1011 | 3.571 | 3.214 | 3.929 | 29.4 | 73.2 | 0.714 |
| 18 | 1101 | 4.286 | 3.929 | 4.643 | 14.7 | 88.7 | 0.857 |
| 20 | 1111 | 5 | 4.643 | | Short | Open | 1.000 |

## APPLICATIONS INFORMATION

### DATA CONVERTERS

The LTC4286 incorporates a pair of 12-bit Σ-Δ ADCs, and a third data converter, which monitors temperature with a 1°C/LSB. One converter continuously samples the current-sense voltage, while the other monitors the input voltage, output voltage, and the $V_{DD}$-SOURCE voltage. The Σ-Δ architecture inherently averages signal noise during the measurement period. The second data converter can be configured to measure $V_{IN}$ at the $V_{DD}$ pin, $V_{OUT}$ at the SOURCE pin, and/or the voltage across the MOSFET by selecting related bits in the MFR_ADC_CONFIG register. The data converter full scale is 32 mV for the current-sense voltage, a choice of 102.4 V or 25.6 V for $V_{DD}$ and $V_{SOURCE}$, 2.56 V for GPIO and 320 mV for the $V_{DD}$-SOURCE measurement.

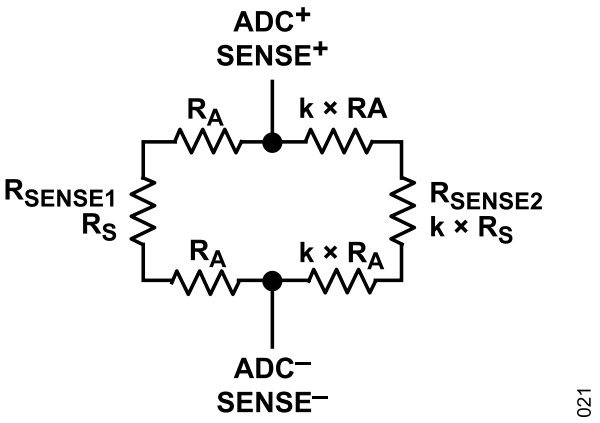


*Figure 20. Weighted Averaging Sense Voltages*

The ADC+ and ADC– input pins allow the ADC to measure the average voltage across the sense resistor. Some applications may use parallel sense resistors to achieve a specific resistance, in which case averaging resistors can be selected with the same ratio as the sense resistors they connect to, which allows the ADC to still measure current accurately. For more details, see Figure 20. In this case, the effective ADC sense resistor is $R_S$ in parallel with k × $R_S$ for the current limit. Scaling the averaging resistors, $R_A$, by the same scaling factor, k, allows the ADC to measure the correct sense voltage for this effective sense resistor. The smallest averaging resistor on the ADC+ or SENSE+ side must not exceed 1 Ω.

The two data converters are synchronized, and after each current measurement conversion, the measured current is multiplied by the measured $V_{DD}$ or $V_{SOURCE}$, as selected by the VPWR_SELECT bit in the MFR_CONFIG1 register, to yield input or output power. The measurements are compared to the min/max warning thresholds and set the corresponding ADC warning bits in the MFR_SYSTEM_STATUS2 register and generate an alert if configured to do so in the MFR_STAT2_ALERT_MASK register.

The following formulas are used to convert the values in the ADC result registers into physical units. The data is in twos complement format, left justified, so for 12-bit data the MSB is always 0, and the 3 LSBs are also 0s.

To calculate the input and output voltage, use the following equation:

$$V = \frac{CODE(WORD) \times V_{FS(OUT)}}{2^{15} - 1} \quad (5)$$

where $V_{FS(OUT)}$ is 25.6 V or 102.4 V, depending on the part being in 25 V or 100 V mode, respectively.

To calculate the current in amperes, use the following equation:

$$I = \frac{CODE(WORD) \times 0.032V}{\left(2^{15} - 1\right) \times R_{SENSE}} \quad (6)$$

To calculate $V_{DD}$ – SOURCE in volts, use the following equation:

$$V = \frac{CODE(WORD) \times 0.32V}{2^{15} - 1} \quad (7)$$

To calculate power in watts, use the following equation:

$$P = \frac{CODE(WORD) \times 0.032V \times V_{FS(OUT)} \times 2^{15}}{\left(2^{15} - 1\right)^2 \times R_{SENSE}} \quad (8)$$

Temperature data is provided in degrees Kelvin, as follows:

T°K = code

T°C = code – 273.15

*Table 6. LTC4286 ADC Measurement Pattern in Continuous Mode, Assuming All AUX Channels Selected*

| Conversions over Time | | | | | |
|---|---|---|---|---|---|
| ADC1 | | ADC1 | ADC1 | | ADC1 |
| (ADC+ – ADC–) | | (ADC+ – ADC–) | (ADC+ – ADC–) | | (ADC+ – ADC–) |
| ADC2 | | ADC2 | ADC2 | | ADC2 |
| $V_{OUT}$ | $V_{IN}$ | $V_{DS}$ | $V_{OUT}$ | $V_{IN}$ | $V_{DS}$ |

## APPLICATIONS INFORMATION

*Table 7. LTC4286 ADC Measurement Pattern in Continuous Mode, Assuming No AUX Channels Selected*

| Conversions over Time | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| ADC1 (ADC+ – ADC−) | | ADC1 (ADC+ – ADC−) | | ADC1 (ADC+ – ADC−) | | ADC1 (ADC+ – ADC−) | | ADC1 (ADC+ – ADC−) | |
| ADC2 | | ADC2 | | ADC2 | | ADC2 | | ADC2 | |
| $V_{OUT}$ | $V_{IN}$ | $V_{OUT}$ | $V_{IN}$ | $V_{OUT}$ | $V_{IN}$ | $V_{OUT}$ | $V_{IN}$ | $V_{OUT}$ | $V_{IN}$ |

PMBus specifies M, B, and R constants for use in calculating ADC results. See Table 8 for the LTC4286 M, B, and R parameters.

*Table 8. PMBus M, B, and R Parameters*

| Parameter | M | R | B |
|---|---|---|---|
| V (102.4 V range) | 32 | 1 | 0 |
| V (25.6 V range) | 128 | 1 | 0 |
| I | 1024 × $R_S$[1] | 3 | 0 |
| P (102.4 V range) | $R_S$ | 4 | 0 |
| P (25.6 V range) | 4 × $R_S$ | 4 | 0 |
| T°C | 1 | 0 | 273.15 |

[1] $R_S$ = value of the current sense resistor in Ω.

Values are calculated as follows:

$$Value = \left(\frac{1}{M}\right) \times Code \times 10^{-R} - B \quad (9)$$

For example, when $R_S$ = 0.333 mΩ,

$$\begin{aligned} &V(code) = 16384 \quad (102.4V \quad range) \\ &V = \frac{1}{32} \times 16384 \times 10^{-1} = 51.2V \\ &I(code) \quad = 16384 \\ &I = \frac{1}{1024/0.333m\Omega} \times 16384 \times 10^{-3} = 48A \\ &P(code) = 8192 \\ &P = \frac{1}{0.333m\Omega} \times 8192 \times 10^{-4} = 2460W \end{aligned} \quad (10)$$

## APPLICATIONS INFORMATION

### SMBUS SERIAL INTERFACE

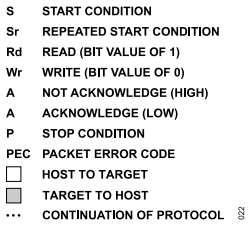


*Figure 21. PMBus Packet Protocol Diagram Element Key*

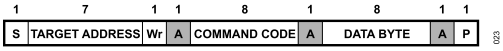


*Figure 22. Write Byte Protocol*

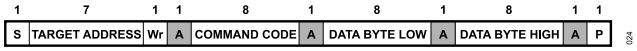


*Figure 23. Write Word Protocol*

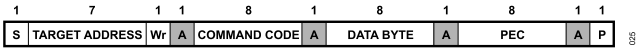


*Figure 24. Write Byte Protocol with PEC*


*Figure 25. Write Word Protocol with PEC*

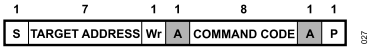


*Figure 26. Send Byte Protocol*

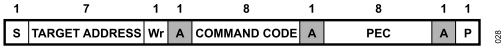


*Figure 27. Send Byte Protocol with PEC*

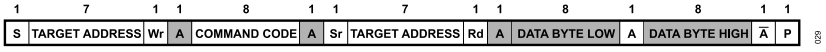


*Figure 28. Read Word Protocol*

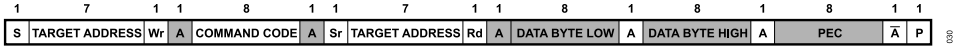


*Figure 29. Read Word Protocol with PEC*


*Figure 30. Read Byte Protocol*

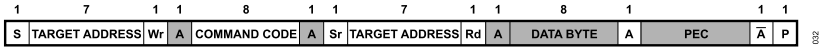


*Figure 31. Read Byte Protocol with PEC*

## APPLICATIONS INFORMATION

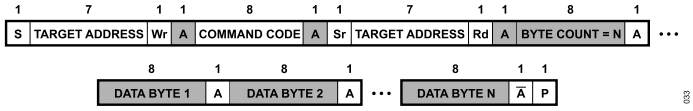


*Figure 32. Block Read*


*Figure 33. Block Read with PEC*

*Table 9. LTC4286 Device Addressing*

| Description | Hex Device Address | | Binary Device Address | | | | | | | | LTC4286 Address Pins[1] | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 7-bit† | 8-bit[2] | 6 | 5 | 4 | 3 | 2 | 1 | 0 | R/W No. | ADR1 | ADR0 |
| Mass Write | 0F | 1E | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | X | X |
| Alert Response | 0C | 19 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | X | X |
| 0 | 40 | 80 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | X | L | L |
| 1 | 41 | 82 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | X | L | NC |
| 2 | 42 | 84 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | X | L | H |
| 3 | 43 | 86 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | X | NC | L |
| 4 | 44 | 88 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | X | NC | NC |
| 5 | 45 | 8A | 1 | 0 | 0 | 0 | 1 | 0 | 1 | X | NC | H |
| 6 | 46 | 8C | 1 | 0 | 0 | 0 | 1 | 1 | 0 | X | H | L |
| 7 | 47 | 8E | 1 | 0 | 0 | 0 | 1 | 1 | 1 | X | H | NC |
| 8 | 11 | 22 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | X | H | H |

[1] H = connect to $INTV_{CC}$, L = connect to GND, NC = no connect or open, and X = do not care.

[2] 8-bit hexadecimal address with LSB R/W bit = 0.

## APPLICATIONS INFORMATION

### PMBUS COMMAND SUMMARY

*Table 10. LTC4286 PMBus Command Summary*

| Command Name | CMD Code | Description | Type[1] | Data Format[2] | Unit[2] | Default Value[2] |
|---|---|---|---|---|---|---|
| PAGE | 0x00 | Any value can be written to PAGE, but the value is not used by the chip internally. The value written can be read back. | R/W byte | Register | N/A | 0x00 |
| OPERATION | 0x01 | This command requests the hot-swap to turn on or off. | R/W byte | Register | N/A | N/A |
| CLEAR_FAULTS | 0x03 | This command clears all latched status bits (all bits shaded in orange or pink in Figure 34). MFR_PMB_STAT and MFR_SD_CAUSE are also cleared by this command. | Send byte | N/A | N/A | N/A |
| WRITE_PROTECT | 0x10 | Protect the device against unintended PMBus modifications. | R/W byte | Register | N/A | 0x00 |
| CAPABILITY | 0x19 | Summary of supported optional PMBus features. | R byte | Register | N/A | 0xD0 |
| VOUT_OV_WARN_LIMIT | 0x42 | Sets the overvoltage warning limit for the voltage at $V_{OUT}$ (SOURCE pin). | R/W word | Direct | V | 0x7FFF |
| VOUT_UV_WARN_LIMIT | 0x43 | Sets the undervoltage warning limit for the voltage at $V_{OUT}$ (SOURCE pin). | R/W word | Direct | V | 0 V, 0x0000 |
| IOUT_OC_FAULT_RESPONSE | 0x47 | Action to be taken by the device when an output overcurrent fault is detected. | R/W byte | Register | N/A | 0xC0 |
| IOUT_OC_WARN_LIMIT | 0x4A | Sets overcurrent warning limit for $I_{OUT}$ ADC reading. | R/W word | Direct | A | 32 mV/$R_{SENSE}$ 0x7FFF |
| OT_FAULT_LIMIT | 0x4F | Sets over temperature fault limit for TEMP ADC reading. | R/W word | Direct | °K | 0x7FFF |
| OT_FAULT_RESPONSE | 0x50 | Action to be taken by the device when an over temperature fault is detected. | R/W byte | Register | N/A | 0x80 |
| OT_WARN_LIMIT | 0x51 | Sets overtemperature warn limit for TEMP ADC reading. | R/W word | Direct | °K | 0x7FFF |
| UT_WARN_LIMIT | 0x52 | Sets undertemperature warn limit for TEMP ADC reading. | R/W word | Direct | °K | 0x0000 |
| VIN_OV_FAULT_RESPONSE | 0x56 | Action to be taken by the device when an input overvoltage fault is detected. | R/W byte | Register | N/A | 0xB8 |
| VIN_OV_WARN_LIMIT | 0x57 | Sets the overvoltage warning limit for the voltage at the $V_{IN}$ ($V_{DD}$ pin). | R/W word | Direct | V | 0x7FFF |
| VIN_UV_WARN_LIMIT | 0x58 | Sets the undervoltage warning limit for the voltage at the $V_{IN}$ ($V_{DD}$ pin). | R/W word | Direct | V | 0 V,0x0000 |
| VIN_UV_FAULT_RESPONSE | 0x5A | Action to be taken by the device when an input undervoltage fault is detected. | R/W byte | Register | N/A | 0xB8 |
| PIN_OP_WARN_LIMIT | 0x6B | Sets overpower warning limit for $P_{IN}$ ADC reading. | R/W word | Direct | W | 3.2768/$R_{SENSE}$ 0x7FFF |
| STATUS_BYTE | 0x78 | One byte summary of the unit's fault condition. | R/W byte | Register | N/A | 0x00 |
| STATUS_WORD | 0x79 | Two byte summary of the unit's fault condition. | R/W1C word | Register | N/A | 0x0000 |
| STATUS_VOUT | 0x7A | Provides status information for faults and warnings related to $V_{OUT}$ (SOURCE pin). | R/W1C byte | Register | N/A | 0x00 |
| STATUS_IOUT | 0x7B | Provides status information for faults and warnings related to $I_{OUT}$. | R/W1C byte | Register | N/A | 0x00 |
| STATUS_INPUT | 0x7C | Provides status information for faults and warnings related to $V_{IN}$ and $P_{IN}$ ($V_{DD}$ pin). | R/W1C byte | Register | N/A | 0x00 |
| STATUS_TEMPERATURE | 0x7D | Provides status information for faults and warnings related to temperature. | R/W1C byte | Register | N/A | 0x00 |

## APPLICATIONS INFORMATION

*Table 10. LTC4286 PMBus Command Summary (Continued)*

| Command Name | CMD Code | Description | Type[1] | Data Format[2] | Unit[2] | Default Value[2] |
|---|---|---|---|---|---|---|
| STATUS_CML | 0x7E | Provides status information for faults and warnings related to communication faults. | R/W1C byte | Register | N/A | 0x00 |
| STATUS_OTHER | 0x7F | Other status faults. | R/W1C byte | Register | N/A | 0x00 |
| STATUS_MFR_SPECIFIC | 0x80 | Provides status information for manufacturer specific faults and warnings. | R/W1C byte | Register | N/A | 0x00 |
| READ _VIN | 0x88 | Reads the input voltage $V_{IN}$ ($V_{DD}$ pin). | R word | Direct | V | N/A |
| READ _VOUT | 0x8B | Reads the output voltage $V_{OUT}$ (SOURCE pin). | R word | Direct | V | N/A |
| READ _IOUT | 0x8C | Reads the output current $I_{OUT}$. | R word | Direct | A | N/A |
| READ _TEMPERATURE_1 | 0x8D | Reads the temperature measured by the device. | R word | Direct | °K | N/A |
| READ _PIN | 0x97 | Reads the calculated input power, $P_{IN}$. | R word | Direct | W | N/A |
| PMBUS_REVISION | 0x98 | PMBus revision supported. Current revision is 1.3. | R byte | Register | N/A | 0x33 |
| MFR_ID | 0x99 | Returns string identifying the manufacturer of the device. | R block 3 bytes | ASC | N/A | LTC |
| MFR_MODEL | 0x9A | Returns string identifying the specific model of the device. | R block 7 bytes | ASC | N/A | LTC4286 |
| MFR_REVISION | 0x9B | Returns string identifying the hardware revision of the device. | R block 1 byte | Binary | N/A | 0x10 |
| IC_DEVICE_ID | 0xAD | Returns string identifying the specific model of the device. | R block 1 byte | ASC | N/A | LTC4286 |
| IC_DEVICE_REV | 0xAE | Returns string identifying the hardware revision of the device. | R block 1 byte | ASC | N/A | 0x10 |
| USER_DATA_00 | 0xB0 | Manufacturer reserved for LTPowerPlay®. | R/W word | Register | N/A | N/A |
| USER_DATA_02 | 0xB2 | OEM reserved. | R/W word | Register | N/A | N/A |
| USER_TIME | 0xB9 | Cleared at power-on reset, increments at the internal tick timer rate. Can be written to set time. | R/W block 6 bytes | Binary | N/A | 0x000000000000 |
| MFR_FLT_CONFIG | 0xD2 | Selects option for FAULT pin output (GPIO). | R/W byte | Register | N/A | 0x00 |
| MFR_FET_FAULT_RESPONSE | 0xD6 | Action to be taken in response to FET bad condition. | R/W byte | Register | N/A | 0x41 |
| MFR_OP_FAULT_RESPONSE | 0xD7 | Selects device response to overpower fault. | R/W word | Register | N/A | 0xFFE0 |
| MFR_ADC_CONFIG | 0xD8 | Configures ADC mode and channels. | R/W byte | Register | N/A | 0x01 |
| MFR_AVG_SEL | 0xD9 | Select ADC averaging rate, also enable display of averaged values in READ_VIN, READ_VOUT, READ_IOUT and READ_PIN commands. | R/W byte | Register | N/A | 0x85 |
| MFR_SYSTEM_STATUS1 | 0xE0 | Provides manufacturer specific status information. | R/W1C word | Register | N/A | N/A |
| MFR_SYSTEM_STATUS2 | 0xE1 | Provides manufacturer system warning information. | R/W1C word | Register | N/A | N/A |
| MFR_PMB_STAT | 0xE2 | Provides detailed status for latest PMBus transfers, which failed. | R/W byte | Register | N/A | 0x00 |
| MFR_PADS_LIVE_STATUS | 0xE5 | State of I/O pads and live status bits. | R word | Register | N/A | N/A |
| MFR_SPECIAL_ID | 0xE7 | This register contains the manufacturer ID, 0x7030 for 4286. | R word | Register | N/A | 0x7030 |
| MFR_COMMON | 0xEF | Manufacturer status bits that are common across multiple LTC chips. | R byte | Register | N/A | N/A |
| MFR_SD_CAUSE | 0xF1 | Cause of last hot-swap shut down. | R byte | Register | N/A | 0x00 |
| MFR_CONFIG1 | 0xF2 | Configures current limit, voltage range for $V_{IN}$ and $V_{OUT}$ and calculated power input. | R/W word | Register | N/A | 0x5572 |
| MFR_CONFIG2 | 0xF3 | Miscellaneous configuration. | R/W word | Register | N/A | 0x00EF |
| MFR_GPIO_INV | 0xF4 | Sets polarity of the GPIO inputs and outputs. | R/W word | Register | N/A | 0x009B |
| MFR_GPO_SEL41 | 0xF5 | Configures the GPIO1, GPIO2, GPIO3, and GPIO4 output functions. | R/W word | Register | N/A | 0x5F43 |

## APPLICATIONS INFORMATION

*Table 10. LTC4286 PMBus Command Summary (Continued)*

| Command Name | CMD Code | Description | Type[1] | Data Format[2] | Unit[2] | Default Value[2] |
|---|---|---|---|---|---|---|
| MFR_GPO_SEL85 | 0xF6 | Configures the GPIO5, GPIO6, GPIO7, and GPIO8 output functions. | R/W word | Register | N/A | 0x8207 |
| MFR_GPI_SEL | 0xF7 | Configures the GPIO1 to GPIO8 input functions. | R/W word | Register | N/A | 0x0005 |
| MFR_GPI_DATA | 0xF8 | Input values for the GPIO1 to GPIO8. | R byte | Register | N/A | N/A |
| MFR_GPO_DATA | 0xF9 | Output values for the GPIO1 to GPIO8. | R/W byte | Register | N/A | 0xFF |
| MFR_REBOOT_CONTROL | 0xFD | Enables reboot and configures initialization options. | R/W byte | Register | N/A | 0x00 |
| MFR_IOUT | 0xFE00 | $I_{OUT}$ value, no averaging. | R word | Direct | A | N/A |
| MFR_IOUT_UC_LIMIT | 0xFE04 | Limit for $I_{OUT}$ undercurrent warning. | R/W word | Direct | A | 0x0000 |
| MFR_IOUT_OC_LIMIT | 0xFE05 | Limit for $I_{OUT}$ overcurrent warning. | R/W word | Direct | A | 0x7FFF |
| MFR_PIN | 0xFE08 | PIN value, no averaging. | R word | Direct | W | N/A |
| MFR_PIN_UP_LIMIT | 0xFE0C | Limit for $P_{IN}$ underpower warning. | R/W word | Direct | W | 0x0000 |
| MFR_PIN_OP_LIMIT | 0xFE0D | Limit for $P_{IN}$ overpower warning. | R/W word | Direct | W | 0x7FFF |
| MFR_VIN | 0xFE10 | $V_{IN}$ value, no averaging. | R word | Direct | V | N/A |
| MFR_VIN_UV_LIMIT | 0xFE14 | Limit for $V_{IN}$ undervoltage warning. | R/W word | Direct | V | 0x0000 |
| MFR_VIN_OV_LIMIT | 0xFE15 | Limit for $V_{IN}$ overvoltage warning. | R/W word | Direct | V | 0x7FFF |
| MFR_VOUT | 0xFE18 | $V_{OUT}$ value, no averaging. | R word | Direct | V | N/A |
| MFR_VOUT_UV_LIMIT | 0xFE1C | Limit for $V_{OUT}$ undervoltage warning. | R/W word | Direct | V | 0x0000 |
| MFR_VOUT_OV_LIMIT | 0xFE1D | Limit for $V_{OUT}$ overvoltage warning. | R/W word | Direct | V | 0x7FFF |
| MFR_VDS | 0xFE20 | $V_{DS}$ value, no averaging. | R word | Direct | V | N/A |
| MFR_VDS_UV_LIMIT | 0xFE24 | Limit for $V_{DS}$ undervoltage warning. | R/W word | Direct | V | 0x0000 |
| MFR_VDS_OV_LIMIT | 0xFE25 | Limit for $V_{DS}$ overvoltage warning. | R/W word | Direct | V | 0x7FFF |
| MFR_TEMP | 0xFE48 | TEMP value, no averaging. | R word | Direct | °K | N/A |
| MFR_TEMP_UT_LIMIT | 0xFE4C | Limit for TEMP undertemperature warning. | R/W word | Direct | °K | 0x0000 |
| MFR_TEMP_OT_LIMIT | 0xFE4D | Limit for TEMP overtemperature warning. | R/W word | Direct | °K | 0x7FFF |
| MFR_PIN_OP1_FAULT_LIMIT | 0xFE58 | Limit for $P_{IN}$ over-power timed fault. | R/W word | Direct | W | 0x7FFF |
| MFR_PIN_OP2_FAULT_LIMIT | 0xFE59 | Limit for $P_{IN}$ over-power immediate fault. | R/W word | Direct | W | 0x7FFF |
| MFR_STATUS_BYTE | 0xFEC0 | One byte summary of the unit's fault condition. | R/W1S byte | Register | N/A | 0x00 |
| MFR_STATUS_WORD_HIGH | 0xFEC1 | Upper byte of STATUS_WORD. | R/W1S byte | Register | N/A | 0x00 |
| MFR_STATUS_VOUT | 0xFEC2 | Provides status information for faults and warnings related to $V_{OUT}$ (SOURCE pin). | R/W1S byte | Register | N/A | 0x00 |
| MFR_STATUS_IOUT | 0xFEC3 | Provides status information for faults and warnings related to $I_{OUT}$. | R/W1S byte | Register | N/A | 0x00 |
| MFR_STATUS_INPUT | 0xFEC4 | Provides status information for faults and warnings related to $V_{IN}$ and $P_{IN}$ ($V_{DD}$ pin). | R/W1S byte | Register | N/A | 0x00 |
| MFR_STATUS_TEMP | 0xFEC5 | Provides status information for faults and warnings related to temperature. | R/W1S byte | Register | N/A | 0x00 |
| MFR_STATUS_CML | 0xFEC6 | Provides status information for faults and warnings related to communication faults. | R/W1S byte | Register | N/A | 0x00 |
| MFR_STATUS_OTHER | 0xFEC7 | Other status faults. | R/W1S byte | Register | N/A | 0x00 |
| MFR_SPECIFIC_STATUS | 0xFEC8 | Provides status information for manufacturer specific faults and warnings. | R/W1S byte | Register | N/A | 0x00 |
| MFR_SYS_STAT1_SET | 0xFECA | Provides manufacturer specific status information. | R/W1S word | Register | N/A | 0x0000 |
| MFR_SYS_STAT2_SET | 0xFECC | Provides manufacturer system warning information. | R/W1S word | Register | N/A | 0x0000 |
| MFR_BYTE_ALERT_MASK | 0xFED0 | Alert mask for STATUS_BYTE. | R/W byte | Register | N/A | 0x80 |
| MFR_VOUT_ALERT_MASK | 0xFED2 | Alert mask for STATUS_VOUT. | R/W byte | Register | N/A | 0x60 |
| MFR_IOUT_ALERT_MASK | 0xFED3 | Alert mask for STATUS_IOUT. | R/W byte | Register | N/A | 0xA0 |
| MFR_INPUT_ALERT_MASK | 0xFED4 | Alert mask for STATUS_INPUT. | R/W byte | Register | N/A | 0xF1 |

## APPLICATIONS INFORMATION

*Table 10. LTC4286 PMBus Command Summary (Continued)*

| Command Name | CMD Code | Description | Type[1] | Data Format[2] | Unit[2] | Default Value[2] |
|---|---|---|---|---|---|---|
| MFR_TEMP_ALERT_MASK | 0xFED5 | Alert mask for STATUS_TEMPERATURE. | R/W byte | Register | N/A | 0xE0 |
| MFR_CML_ALERT_MASK | 0xFED6 | Alert mask for STATUS_CML. | R/W byte | Register | N/A | 0xE3 |
| MFR_SPECIFIC_ALERT_MASK | 0xFED8 | Alert mask for STATUS_MFR_SPECIFIC. | R/W byte | Register | N/A | 0xFF |
| MFR_STAT1_ALERT_MASK | 0xFEDA | Alert mask for MFR_SYSTEM_STATUS1. | R/W word | Register | N/A | 0x3CFE |
| MFR_STAT2_ALERT_MASK | 0xFEDC | Alert mask for MFR_SYSTEM_STATUS2. | R/W word | Register | N/A | 0xCFFF |

1 R = read only, R/W = read or write, R/W1C = read or write 1s to clear, and R/W1S = read or write 1s to set.

2 N/A = not applicable.

## APPLICATIONS INFORMATION

### ADC-RELATED COMMANDS AND ALIASES

PMBus defines command codes for several ADC values and warning limits. The LTC4286 uses these command codes, which are defined. Many additional ADC-related commands are not defined as PMBus standard.

The MFR command area above 0xFE00 is arranged orthogonally to allow addressing ADC-related values, both PMBus standard and LTC4286 specific. This leads to multiple command names for the same internal register in many cases. Results are the same whether a PMBus standard command or its MFR alias is accessed.

The five READ_ PMBus standard commands respond with either averaged or non-averaged ADC data. This depends on the setting of DISP_AVG in MFR_AVG_SEL. In the MFR area, non-averaged ADC results are available at any time at separate commands.

*Table 11. PMBus ADC-Related Commands and MFR Aliases*

| PMBus Command | Code | MFR Alias | Code |
|---|---|---|---|
| VOUT_OV_WARN_LIMIT | 0x42 | MFR_VOUT_OV_LIMIT | 0xFE1D |
| VOUT_UV_WARN_LIMIT | 0x43 | MFR_VOUT_UV_LIMIT | 0xFE1C |
| IOUT_OC_WARN_LIMIT | 0x4A | MFR_IOUT_OC_LIMIT | 0xFE05 |
| OT_WARN_LIMIT | 0x51 | MFR_TEMP_OT_LIMIT | 0xFE4D |
| UT_WARN_LIMIT | 0x52 | MFR_TEMP_UT_LIMIT | 0xFE4C |
| VIN_OV_WARN_LIMIT | 0x57 | MFR_VIN_OV_LIMIT | 0xFE15 |
| VIN_UV_WARN_LIMIT | 0x58 | MFR_VIN_UV_LIMIT | 0xFE14 |
| PIN_OP_WARN_LIMIT | 0x6B | MFR_PIN_OP_LIMIT | 0xFE0D |
| READ_VIN | 0x88 | MFR_VIN | 0xFE10 |
| READ_VOUT | 0x8B | MFR_VOUT | 0xFE18 |
| READ_IOUT | 0x8C | MFR_IOUT | 0xFE00 |
| READ_TEMPERATURE_1 | 0x8D | MFR_TEMP | 0xFE48 |
| READ_PIN | 0x97 | MFR_PIN | 0xFE08 |

*Table 12. OPERATION (0x01) R/W*

| Bit | Name | Default | Operation |
|---|---|---|---|
| 7 | ON Bit | Not applicable | Indicates On/Off Command of FET, 1 = FET Commanded On, 0 = FET Commanded Off. A 0-to-1 edge for this bit clears all orange and pink shaded bits in Figure 34. At power-up reset or reboot, the ON bit is selected based on the CFIG6 input. EN must also be high to turn on. |
| [6:0] | Reserved | 0000000 | Always returns 0000000. |

*Table 13. WRITE_PROTECT (0x10) R/W*

| Bit | Name | Default | Operation |
|---|---|---|---|
| 7 | WP1 | 0 | Disables all writes except WRITE_PROTECT and PAGE commands, 1 = disable writes, 0 = enable writes. |
| 6 | WP2 | 0 | Disables all writes except WRITE_PROTECT, PAGE, OPERATION, and CLEAR_FAULTS commands, 1 = disable writes, 0 = enable writes. |
| [5:0] | Reserved | 000000 | Always returns 00000. |

*Table 14. CAPABILITY (0x19) Read Only*

| Bit | Name | Default | Operation |
|---|---|---|---|
| 7 | PEC | 1 | Indicates that PEC supported. |
| [6:5] | MAX_BUS_SPEED | 10 | Indicates that 1 MHz max bus speed supported. |
| 4 | SMBALERT# | 1 | Indicates that SMBus Alert response supported. |
| 3 | IEEE | 0 | Indicates that numeric data is linear or direct format. |
| 2 | AVSBUS | 0 | Indicates that AVSBus not supported. |
| [1:0] | Reserved | 00 | Always returns 00. |

## APPLICATIONS INFORMATION

*Table 15. IOUT_OC_FAULT_RESPONSE (0x47) R/W*

| Bit | Name | Default | Operation | |
|---|---|---|---|---|
| [7:6] | OC_FAULT_RESPONSE | 11 | Configures Response options for OC fault. | |
| | | | **Value** | **Meaning** |
| | | | 00 | Ignore fault. |
| | | | 11 | Device shuts down and responds according to retry settings. |
| [5:3] | OC_FAULT_RETRY | 000 | Configures Retry options for OC fault. | |
| | | | **Value** | **Meaning** |
| | | | 000 | Latchoff |
| | | | 001 | 1 retry |
| | | | 010 | 2 retries |
| | | | 011 | 3 retries |
| | | | 100 | 4 retries |
| | | | 101 | 5 retries |
| | | | 110 | 6 retries |
| | | | 111 | ∞ retries |
| [2:0] | Reserved | 000 | Always returns 000. | |

*Table 16. OT_FAULT_RESPONSE (0x50) R/W*

| Bit | Name | Default | Operation | |
|---|---|---|---|---|
| [7:6] | OT_FAULT_RESPONSE | 10 | Configures Response options for OT fault. | |
| | | | **Value** | **Meaning** |
| | | | 00 | Ignore fault. |
| | | | 10 | Device shuts down and responds according to retry settings. |
| [5:3] | OT_FAULT_RETRY | 000 | Configures Retry options for OT fault. | |
| | | | **Value** | **Meaning** |
| | | | 000 | Latchoff |
| | | | 001 | 1 retry |
| | | | 010 | 2 retries |
| | | | 011 | 3 retries |
| | | | 100 | 4 retries |
| | | | 101 | 5 retries |
| | | | 110 | 6 retries |
| | | | 111 | ∞ retries |
| [2:0] | Reserved | 000 | Always returns 000. | |

*Table 17. VIN_OV_FAULT_RESPONSE (0x56) R/W*

| Bit | Name | Default | Operation | |
|---|---|---|---|---|
| [7:6] | VIN_OV_FAULT_RESPONSE | 10 | Configures Response options for OV fault. | |
| | | | **Value** | **Meaning** |
| | | | 00 | Ignore fault. |
| | | | 10 | Device shuts down and responds according to retry settings. |
| [5:3] | VIN_OV_FAULT_RETRY | 111 | Configures Retry options for OV fault. | |
| | | | **Value** | **Meaning** |
| | | | 000 | Latchoff |
| | | | 001 | 1 retry |
| | | | 010 | 2 retries |

## APPLICATIONS INFORMATION

*Table 17. VIN_OV_FAULT_RESPONSE (0x56) R/W (Continued)*

| Bit | Name | Default | Operation | |
|---|---|---|---|---|
| | | | 011 | 3 retries |
| | | | 100 | 4 retries |
| | | | 101 | 5 retries |
| | | | 110 | 6 retries |
| | | | 111 | ∞ retries |
| [2:0] | Reserved | 000 | Always returns 000. | |

*Table 18. VIN_UV_FAULT_RESPONSE (0x5A) R/W*

| Bit | Name | Default | Operation | |
|---|---|---|---|---|
| [7:6] | VIN_UV_FAULT_RESPONSE | 10 | Configures Response options for UV fault. | |
| | | | **Value** | **Meaning** |
| | | | 00 | Ignore fault. |
| | | | 10 | Device shuts down and responds according to retry settings. |
| [5:3] | VIN_UV_FAULT_RETRY | 111 | Configures Retry options for UV fault. | |
| | | | **Value** | **Meaning** |
| | | | 000 | Latchoff |
| | | | 001 | 1 retry |
| | | | 010 | 2 retries |
| | | | 011 | 3 retries |
| | | | 100 | 4 retries |
| | | | 101 | 5 retries |
| | | | 110 | 6 retries |
| | | | 111 | ∞ retries |
| [2:0] | Reserved | 000 | Always returns 000. | |

## APPLICATIONS INFORMATION

### STATUS REGISTER SUMMARY

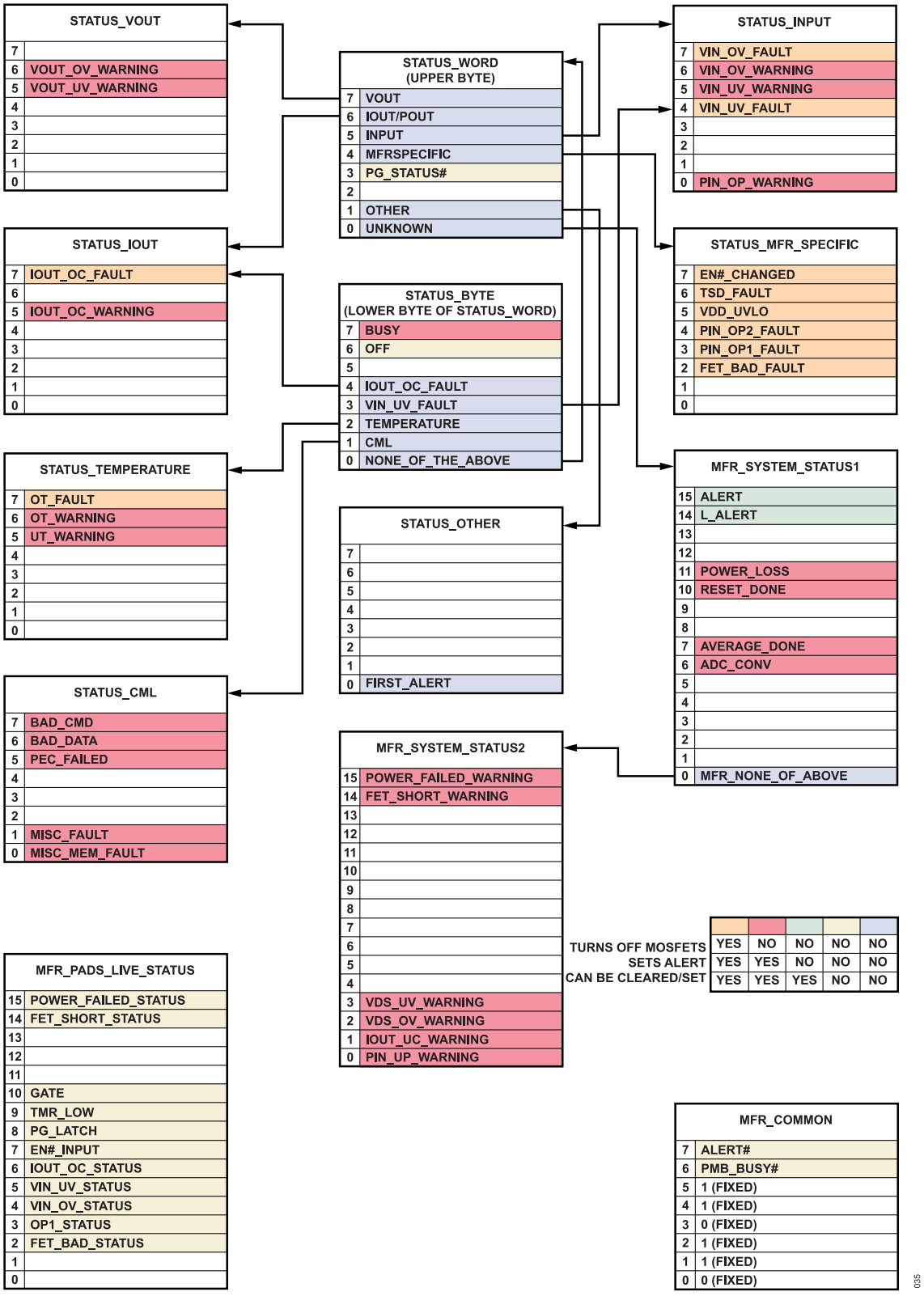


*Figure 34. LTC4286 Status Register Summary*

## APPLICATIONS INFORMATION

### LATCHED STATUS AND MASK COMMANDS

#### Overview

Latched status is kept in the following command locations:

- STATUS_BYTE
- STATUS_WORD
- STATUS_VOUT
- STATUS_IOUT
- STATUS_INPUT
- STATUS_TEMPERATURE
- STATUS_CML
- STATUS_OTHER
- STATUS_MFR_SPECIFIC
- MFR_SYSTEM_STATUS1
- MFR_SYSTEM_STATUS2

The status bits have three categories:

- Faults: conditions that cause GATE to turn off.
- Warnings: conditions, which can lead to a fault.
- Events: errors and other information, not related to faults.

Once set, each status bit remains set until one of the following occurs:

- A chip reset or reboot.
- A CLEAR_FAULTS command clears them all.
- The ON bit in the OPERATION command is cleared then set again.
- At an active edge of EN, all status bits are cleared if RESET_FAULT_ENABLE is set in MFR_CONFIG2.
- A 1 bit is written to the corresponding location in the status command to clear it.

The LTC4286 also provides a method for software to set latched status bits. To support this, a parallel list of commands is defined. Writing a 1 bit to these commands set the corresponding status bits.

Each of the latched status bits is able to generate an SMBus alert condition by pulling down on a selected open-drain output (for more details, see Table 19).

Status bits are combined with corresponding mask bits before activating the alert. If the mask bit is 1, the status bit does not contribute to the alert. The LTC4286 power-on default is for all status bits to be masked off, preventing alert indication. Software can write the mask commands to unmask selected status bits.

Table 19 shows how the commands for latched status are related.

***Table 19. Latched Status Commands***

| Main (R/W1C) | Code | Mirror (R/W1S) | Code | Mask (R/W)[1] | Code[1] |
|---|---|---|---|---|---|
| STATUS_BYTE | 0x78 | MFR_STATUS_BYTE | 0xFEC0 | MFR_BYTE_ALERT_MASK | 0xFED0 |
| STATUS_WORD | 0x79 | MFR_STATUS_BYTE | 0xFEC0 | MFR_BYTE_ALERT_MASK | 0xFED0 |
| | | MFR_STATUS_WORD_HIGH | 0xFEC1 | | |
| STATUS_VOUT | 0x7A | MFR_STATUS_VOUT | 0xFEC2 | MFR_VOUT_ALERT_MASK | 0xFED2 |
| STATUS_IOUT | 0x7B | MFR_STATUS_IOUT | 0xFEC3 | MFR_IOUT_ALERT_MASK | 0xFED3 |
| STATUS_INPUT | 0x7C | MFR_STATUS_INPUT | 0xFEC4 | MFR_INPUT_ALERT_MASK | 0xFED4 |
| STATUS_TEMPERATURE | 0x7D | MFR_STATUS_TEMP | 0xFEC5 | MFR_TEMP_ALERT_MASK | 0xFED5 |
| STATUS_CML | 0x7E | MFR_STATUS_CML | 0xFEC6 | MFR_CML_ALERT_MASK | 0xFED6 |
| STATUS_OTHER | 0x7F | MFR_STATUS_OTHER | 0xFEC7 | N/A | N/A |
| STATUS_MFR_SPECIFIC | 0x80 | MFR_SPECIFIC_STATUS | 0xFEC8 | MFR_SPECIFIC_ALERT_MASK | 0xFED8 |
| MFR_SYSTEM_STATUS1 | 0xE0 | MFR_SYS_STAT1_SET | 0xFECA | MFR_STAT1_ALERT_MASK | 0xFEDA |
| MFR_SYSTEM_STATUS2 | 0xE1 | MFR_SYS_STAT2_SET | 0xFECC | MFR_STAT2_ALERT_MASK | 0xFEDC |

[1] N/A = not applicable.

***Table 20. STATUS_BYTE (0x78) W1C, MFR_STATUS_BYTE (0xFEC0) W1S, MFR_BYTE_ALERT_MASK (0xFED0) R/W***

| Bit | Name | Default 0x78, 0xFEC0 | Default 0xFED0 | Operation |
|---|---|---|---|---|
| 7 | BUSY | 0 | 1 | Bit set if the device was busy and cannot respond to a PMBus access. |
| 6 | OFF | 0 | RO/0 | Hot-swap gate is off, 1 = gate is disabled, 0 = gate is enabled. |
| 5 | Reserved | 0 | RO/0 | Always returns 0. |
| 4 | IOUT_OC_FAULT | 0 | RO/0 | Copy of IOUT_OC_FAULT bit in STATUS_IOUT. |

## APPLICATIONS INFORMATION

*Table 20. STATUS_BYTE (0x78) W1C, MFR_STATUS_BYTE (0xFEC0) W1S, MFR_BYTE_ALERT_MASK (0xFED0) R/W (Continued)*

| Bit | Name | Default 0x78, 0xFEC0 | Default 0xFED0 | Operation |
|---|---|---|---|---|
| 3 | VIN_UV_FAULT | 0 | RO/0 | Copy of VIN_UV_FAULT in STATUS_VIN. |
| 2 | TEMPERATURE | 0 | RO/0 | Temperature fault or warning, 1 = there are one or more active status bits in the STATUS_TEMPERATURE (7D), 0 = There are no active status bits. |
| 1 | CML | 0 | RO/0 | CML fault or warning, 1 = there are one or more active status bits in the STATUS_CML (7E), 0 = There are no active status bits. |
| 0 | NONE_OF_THE_ABOVE | 0 | RO/0 | None of the above, 1 = one or more status bits not listed in bits [7:1] are set. |

*Table 21. STATUS_WORD (0x79) R/W1C, MFR_STATUS_BYTE/MFR_STATUS_WORD_HIGH (0xFEC0/0xFEC1) R/W1S, MFR_BYTE_ALERT_MASK (0xFED0) R/W*

| Bit | Name | Default 0x79, 0xFEC0 | Default 0xFED0 (Byte Register) | Operation |
|---|---|---|---|---|
| 15 | VOUT | 0 | N/A | $V_{OUT}$ (SOURCE pin) fault or warning, 1 = there are one or more active status bits in the STATUS_VOUT (0X7A), 0 = There are no active status bits. |
| 14 | IOUT | 0 | N/A | $I_{OUT}$ current fault or warning, 1 = there are one or more active status bits in the STATUS_IOUT (0X7B), 0 = There are no active status bits. |
| 13 | INPUT | 0 | N/A | $V_{IN}$ ($V_{DD}$ pin) status warning, 1 = there are one or more active status bits in the STATUS_INPUT (0x7C), 0 = There are no active status bits. |
| 12 | MFRSPECIFIC | 0 | N/A | Manufacture specific fault or warning, 1 = there are one or more active faults, bits [7:3] in the STATUS_MFR_SPECIFIC (0x80), 0 = There are no active fault bits. |
| 11 | PG_STATUS# | 0 | N/A | Bit is high if FB input pin is below 2.56 V, indicating the MOSFET output voltage is not high enough for PG_LATCH status. |
| 10 | Reserved | 0 | N/A | Always returns 0. |
| 9 | OTHER | 0 | N/A | Status is present in STATUS_OTHER byte. |
| 8 | UNKNOWN | 0 | N/A | Bit is high to indicate one or more bits in MFR_SYSTEM_STATUS1 are set. |
| 7 | BUSY | 0 | 1 | Bit set if the device was busy and could not respond to a PMBus access. |
| 6 | OFF | 0 | RO/0 | Hot-swap gate is off, 1 = gate is disabled, 0 = gate is enabled. |
| 5 | Reserved | 0 | RO/0 | Always returns 0. |
| 4 | IOUT_OC_FAULT | 0 | RO/0 | Copy of IOUT_OC_FAULT bit in STATUS_IOUT. |
| 3 | VIN_UV_FAULT | 0 | RO/0 | Copy of VIN_UV_FAULT in STATUS_VIN. |
| 2 | TEMPERATURE | 0 | RO/0 | Temperature fault or warning, 1 = there are one or more active status bits in the STATUS_TEMPERATURE (7Dh), 0 = There are no active status bits. |
| 1 | CML | 0 | RO/0 | CML fault or warning, 1 = there are one or more active status bits in the STATUS_CML (7Eh), 0 = There are no active status bits. |
| 0 | NONE_OF_THE_ABOVE | 0 | RO/0 | None of the above, 1 = one or more status bits not listed in bits [7:1] are set. |

*Table 22. STATUS_VOUT (0x7A) R/W1C, MFR_STATUS_VOUT (0xFEC2) R/W1S, MFR_VOUT_ALERT_MASK (0xFED2) R/W*

| Bit | Name | Default 0x7A, 0xFEC2 | Default 0xFED2 | Operation |
|---|---|---|---|---|
| 7 | Reserved | 0 | RO/0 | Always returns 0. |
| 6 | VOUT_OV_WARNING | 0 | 1 | $V_{OUT}$ overvoltage warning, 1 = detected overvoltage by the VOLTAGE ADC measuring the SOURCE pin, 0 = no OV detected. |
| 5 | VOUT_UV_WARNING | 0 | 1 | $V_{OUT}$ undervoltage warning, 1 = detected undervoltage by the VOLTAGE ADC measuring the SOURCE pin, 0 = no UV detected. |
| [4:0] | Reserved | 00000 | RO/00000 | Always returns 00000. |

## APPLICATIONS INFORMATION

*Table 23. STATUS_IOUT (0x7B) R/W1C, MFR_STATUS_IOUT (0xFEC3) R/W1S, MFR_IOUT_ALERT_MASK (0xFED3) R/W*

| Bit | Name | Default 0x7B, 0xFEC3 | Default 0xFED3 | Operation |
|---|---|---|---|---|
| 7 | IOUT_OC_FAULT | 0 | 1 | $I_{OUT}$ overcurrent fault (latched), 1 = detected overcurrent past the TMR pin time limit, 0 = no OC fault detected. |
| 6 | Reserved | 0 | RO/0 | Always returns 0. |
| 5 | IOUT_OC_WARNING | 0 | 1 | $I_{OUT}$ overcurrent warning, 1 = detected overcurrent warning by the CURRENT ADC ($V_{SENSE+}$ – $V_{SENSE–}$), 0 = no OC detected. |
| [4:0] | Reserved | 00000 | RO/00000 | Always returns 00000. |

*Table 24. STATUS_INPUT (0x7C) R/W1C, MFR_STATUS_INPUT (0xFEC4) R/W1S, MFR_INPUT_ALERT_MASK (0xFED4) R/W*

| Bit | Name | Default 0x7C, 0xFEC4 | Default 0xFED4 | Operation |
|---|---|---|---|---|
| 7 | VIN_OV_FAULT | 0 | 1 | $V_{IN}$ overvoltage fault (latched), 1 = detected overvoltage on the OV pin, 0 = no OV detected. |
| 6 | VIN_OV_WARNING | 0 | 1 | $V_{IN}$ overvoltage warning, 1 = detected overvoltage by the VOLTAGE ADC measuring the $V_{DD}$ pin, 0 = no OV detected. |
| 5 | VIN_UV_WARNING | 0 | 1 | $V_{IN}$ undervoltage warning, 1 = detected overvoltage by the VOLTAGE ADC measuring the $V_{DD}$ pin, 0 = no UV detected. |
| 4 | VIN_UV_FAULT | 0 | 1 | $V_{IN}$ undervoltage fault (latched), 1 = detected undervoltage on the UV pin, 0 = no UV detected. |
| [3:1] | Reserved | 000 | RO/000 | Always returns 000. |
| 0 | PIN_OP_WARNING | 0 | 1 | Calculated input power, $P_{IN}$, overpower warning, 1 = detected overpower, 0 = no OP detected. |

*Table 25. STATUS_TEMPERATURE (0x7D) R/W1C, MFR_STATUS_TEMP (0xFEC5) R/W1S, MFR_TEMP_ALERT_MASK (0xFED5) R/W*

| Bit | Name | Default 0x7D, -xFED5 | Default 0xFED5 | Operation |
|---|---|---|---|---|
| 7 | OT_FAULT | 0 | 1 | Overtemperature fault (latched), 1 = detected overtemperature fault by the TEMP ADC, 0 = no OT detected. |
| 6 | OT_WARNING | 0 | 1 | Overtemperature warning, 1 = detected overtemperature warning by the TEMP ADC, 0 = no OT detected. |
| 5 | UT_WARNING | 0 | 1 | Undertemperature warning, 1 = detected undertemperature warning by the TEMP ADC, 0 = no UT detected. |
| [4:0] | Reserved | 00000 | RO/00000 | Always returns 00000. |

*Table 26. STATUS_CML (0x7E) R/W1C, MFR_STATUS_CML (0xFEC6) R/W1S, MFR_CML_ALERT_MASK (0xFED6), R/W*

| Bit | Name | Default 0x7E, 0xFEC6 | Default 0xFED6 | Operation |
|---|---|---|---|---|
| 7 | BAD_CMD | 0 | 1 | Invalid or unsupported command received. |
| 6 | BAD_DATA | 0 | 1 | Invalid or unsupported data received. |
| 5 | PEC_FAILED | 0 | 1 | Packet error check failed, or PEC byte missing where is it required. |
| 4 | Reserved | 0 | 0 | Always returns 0. |
| [3:2] | Reserved | 00 | RO/00 | Always returns 00. |
| 1 | MISC_FAULT | 0 | 1 | Miscellaneous communications fault has occurred. |
| 0 | Reserved | 0 | 1 | Reserved |

*Table 27. STATUS_OTHER (0x7F) R/W1C, MFR_STATUS_OTHER (0xFED7) R/W1S*

| Bit | Name | Default | Operation |
|---|---|---|---|
| [7:1] | Reserved | 000000 | Always returns 0000000. |
| 0 | FIRST_ALERT | 0 | Bit set if this chip is the first to assert ALERT# low. |

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*Table 28. STATUS_MFR_SPECIFIC (0x80) R/W1C, MFR_SPECIFIC_STATUS (0xFEC8) R/W1S, MFR_SPECIFIC_ALERT_MASK (0xFED8) R/W*

| Bit | Name | Default 0x80, 0xFEC8 | Default 0xFED8 | Operation |
|---|---|---|---|---|
| 7 | EN_CHANGED | 0 | 1 | Indicates that the EN pin changed state; 1 = EN changed state, 0 = EN unchanged. |
| 6 | TSD_FAULT | 0 | 1 | Latched to a 1 if a thermal shutdown condition is detected, 0 = no thermal shutdown. |
| 5 | VDD_UVLO | 0 | 1 | Latched to a 1 if the $V_{DD}$ input goes below the $V_{DD\_UVLO}$ limit, 0 = no UVLO condition on $V_{DD}$. |
| 4 | PIN_OP2_FAULT | 0 | 1 | Indicates that the $P_{IN}$ has exceeded the limit for immediate fault. |
| 3 | PIN_OP1_FAULT | 0 | 1 | Indicates that the timer has expired for the timed $P_{IN}$ fault limit. |
| 2 | FET_BAD_FAULT | 0 | 1 | Latched to a 1 if FET Bad Fault occurred, 0 = No FET Bad fault. |
| 1 | Reserved | 0 | 1 | Reserved for future use. |
| 0 | Reserved | 0 | 1 | Reserved for future use. |

*Table 29. MFR_FLT_CONFIG (0xD2) R/W*

| Bit | Name | Default | Operation |
|---|---|---|---|
| 1 | OP_TO_FAULT | 0 | Set to gate overpower fault to the FLT output. |
| 0 | OT_TO_FAULT | 0 | Set to gate overtemperature fault to the FLT output. |

*Table 30. MFR_FET_FAULT_RESPONSE (0xD6) R/W*

| Bit | Name | Default | Operation | |
|---|---|---|---|---|
| [7:6] | FET_BAD_RESPONSE | 01 | Configures Response options for FET bad fault. | |
| | | | **Value** | **Meaning** |
| | | | 00 | Ignore fault. |
| | | | 01 | Device continues for FET_BAD FLT DL. If fault still present, then responds according to retry settings. |
| [5:3] | FET_BAD_RETRY | 000 | Configures Retry options for FET bad fault. | |
| | | | **Value** | **Warning** |
| | | | 000 | Latchoff |
| | | | 001 | 1 retry |
| | | | 010 | 2 retries |
| | | | 011 | 3 retries |
| | | | 100 | 4 retries |
| | | | 101 | 5 retries |
| | | | 110 | 6 retries |
| | | | 111 | ∞ retries |
| [2:0] | Reserved | 001 | Reserved for future use, always write 001. | |

*Table 31. MFR_OP_FAULT_RESPONSE (0xD7) R/W*

| Bit | Name | Default | Operation | |
|---|---|---|---|---|
| [15:5] | OP_TIMER | 11111111111 | Timer for OP1 fault. The timer function combines increment and decrement. Each time that $P_{IN}$ is greater than MFR_PIN_OP1_FAULT_LIMIT, an internal counter increments by 2. Each time $P_{IN}$ is less than MFR_PIN_OP1_FAULT_LIMIT that counter decrements by 1. PIN_OP1_FAULT is set if the overpower condition persists for OP_TIMER x 1.13 ms. | |
| [4:3] | OP_FAULT_RESPONSE | 00 | Configures Response options for OP1 or OP2 fault. | |
| | | | **Value** | **Meaning** |

## APPLICATIONS INFORMATION

*Table 31. MFR_OP_FAULT_RESPONSE (0xD7) R/W (Continued)*

| Bit | Name | Default | Operation | |
|---|---|---|---|---|
| | | | 00 | Ignore fault. |
| | | | 10 | Device shut down and responds accordingly to retry settings. |
| [2:0] | OP_FAULT_RETRY | 000 | Configures Retry options for OP1 or OP2 fault. | |
| | | | **Value** | **Meaning** |
| | | | 000 | Latchoff |
| | | | 001 | 1 retry |
| | | | 010 | 2 retries |
| | | | 011 | 3 retries |
| | | | 100 | 4 retries |
| | | | 101 | 5 retries |
| | | | 110 | 6 retries |
| | | | 111 | ∞ retries |

*Table 32. MFR_ADC_CONFIG (0xD8) R/W*

| Bit | Name | Default | Operation |
|---|---|---|---|
| 7 | Reserved | 0 | Reserved for future use. Only write 0. |
| 6 | Reserved | 0 | Always returns 0. |
| 5 | Reserved | 0 | Reserved for future use. Only write 0. |
| 4 | Reserved | 0 | Reserved for future use. Only write 0. |
| 3 | Reserved | 0 | Reserved for future use. Only write 0. |
| 2 | Reserved | 0 | Reserved for future use. Only write 0. |
| 1 | VDS_SELECT | 0 | Enables $V_{DS}$ as an Auxiliary Input for ADC Measurement. |
| 0 | VIN_VOUT_SELECT | 1 | Enables $V_{IN}$ or $V_{OUT}$ as an auxiliary input for ADC Measurement. The choice between the two depends on VPWR_SELECT in MFR_CONFIG1. If $V_{IN}$ is selected in VPWR_SELECT, then $V_{OUT}$ is available as an auxiliary input. In the opposite case, $V_{IN}$ is available as an auxiliary input. |

*Table 33. MFR_AVG_SEL (0xD9) R/W*

| Bit | Name | Default | Operation |
|---|---|---|---|
| 7 | DISP_AVG | 1 | 1 selects averaged values for READ_VIN, READ_VOUT, READ_IOUT and READ_PIN, 0 selects unaveraged values. |
| [6:4] | Reserved | 000 | Always returns 000. |
| [3:0] | ADC_AVERAGE_SELECT | 0101 | Selects number of ADC samples per average. For more details, see Table 34. |

*Table 34. ADC_AVERAGE_SELECT Options*

| Value | Samples | Average Time |
|---|---|---|
| 0000 | 2 | 0.566 ms |
| 0001 | 4 | 1.13 ms |
| 0010 | 8 | 2.27 ms |
| 0011 | 16 | 4.53 ms |
| 0100 | 32 | 9.06 ms |
| 0101 | 64 | 18.1 ms |
| 0110 | 128 | 36.3 ms |
| 0111 | 256 | 72.5 ms |
| 1000 | 512 | 145 ms |
| 1001 | 1024 | 290 ms |
| 1010 | 2048 | 580 ms |
| 1011 | 4096 | 1.16 sec |

## APPLICATIONS INFORMATION

*Table 34. ADC_AVERAGE_SELECT Options (Continued)*

| Value | Samples | Average Time |
|---|---|---|
| 1100 | 8192 | 2.32 sec |
| 1101 | 16384 | 4.64 sec |
| 1110 | 32768 | 9.28 sec |
| 1111 | 65536 | 18.6 sec |

*Table 35. MFR_SYSTEM_STATUS1 (0xE0) R/W1C, MFR_SYS_STAT1_SET (0xFECA) R/W1S, MFR_STAT_ALERT_MASK (0xFEDA) R/W*

| Bit | Name | Default 0xE0, 0xFECA | Default 0xFEDA | Operation |
|---|---|---|---|---|
| 15 | ALERT | 0 | RO/0 | Bit set to 1 when an Alert is generated. This can be cleared via SMBus write or alert response protocol. The bit can be configured to appear as active low or high on any GPIO pin. |
| 14 | L_ALERT | 0 | RO/0 | Alternate version of ALERT or latched ALERT. This bit is set by the same conditions that set ALERT. But it can only be cleared by an SMBus write. This bit can be configured to appear on any GPIO pin as L_ALERT# or L_ALERT. |
| 13 | Reserved | 0 | 1 | Reserved |
| 12 | Reserved | 0 | 1 | Reserved |
| 11 | POWER_LOSS | 0 | 1 | Bit is 1 following a power-on reset, or 0 after a reboot-generated reset. |
| 10 | RESET_DONE | 0 | 1 | Latched status bit is set after each chip reset (either power-on or reboot). |
| [9:8] | Reserved | 00 | RO/00 | Always returns 00. |
| 7 | AVERAGE_DONE | 0 | 1 | Set at the completion of an average. |
| 6 | ADC_CONV | 0 | 1 | Latched to 1 when a full ADC conversion (current and voltage) completes. |
| 5 | Reserved | 0 | 1 | Reserved |
| 4 | Reserved | 0 | 1 | Reserved |
| 3 | Reserved | 0 | 1 | Reserved |
| 2 | Reserved | 0 | 1 | Reserved |
| 1 | Reserved | 0 | 1 | Reserved |
| 0 | MFR_NONE_OF_ABOVE | 0 | RO/0 | Bit is set if bits in MFR_SYSTEM_STATUS2 are set. |

*Table 36. MFR_SYSTEM_STATUS2 (9xE1) R/W1C, MFR_SYS_STAT2_SET (0xFECC) R/W1S, MFR_STAT2_ALERT_MASK (0xFEDC) R/W*

| Bit | Name | Default 0xE1, 0xFECC | Default 0xFEDC | Operation |
|---|---|---|---|---|
| 15 | POWER_FAILED_WARNING | 0 | 1 | This latched bit is set if POWER_FAILED_STATUS goes active. This happens if the FB input pin goes below 2.56 V while the PG_LATCH status bit is set. That indicates a loss of output voltage after it was initially good. |
| 14 | FET_SHORT_WARNING | 0 | 1 | Latched to a 1 if measured ($V_{SENSE+}$ – $V_{SENSE-}$) exceeds 2 mV while FET is off (FET Short was detected); 1 = FET Short Fault occurred, 0 = No FET Short fault. |
| [13:12] | Reserved | 00 | RO/00 | Always returns 00. |
| 11 | Reserved | 0 | 1 | Reserved for future use. Only write 0. |
| 10 | Reserved | 0 | 1 | Reserved for future use. Only write 0. |
| 9 | Reserved | 0 | 1 | Reserved for future use. Only write 0. |
| 8 | Reserved | 0 | 1 | Reserved for future use. Only write 0. |
| 7 | Reserved | 0 | 1 | Reserved for future use. Only write 0. |
| 6 | Reserved | 0 | 1 | Reserved for future use. Only write 0. |
| 5 | Reserved | 0 | 1 | Reserved for future use. Only write 0. |
| 4 | Reserved | 0 | 1 | Reserved for future use. Only write 0. |
| 3 | VDS_UV_WARNING | 0 | 1 | Latched to 1 when the $V_{DS}$ input is below MFR_VDS_MIN_WARN_LIMIT. |
| 2 | VDS_OV_WARNING | 0 | 1 | Latched to 1 when the $V_{DS}$ input is above MFR_VDS_MAX_WARN_LIMIT. |

## APPLICATIONS INFORMATION

*Table 36. MFR_SYSTEM_STATUS2 (9xE1) R/W1C, MFR_SYS_STAT2_SET (0xFECC) R/W1S, MFR_STAT2_ALERT_MASK (0xFEDC) R/W (Continued)*

| Bit | Name | Default 0xE1, 0xFECC | Default 0xFEDC | Operation |
|---|---|---|---|---|
| 1 | IOUT_UC_WARNING | 0 | 1 | Indicates that the $I_{OUT}$ current is below warning limit in MFR_IOUT_UC_WARN_LIMIT. |
| 0 | PIN_UP_WARNING | 0 | 1 | Indicates that the $P_{IN}$ power is below warning limit in MFR_PIN_UP_WARN_LIMIT. |

*Table 37. MFR_PMB_STAT (0xE2) R/W*

| Bit | Name | Operation |
|---|---|---|
| [7:5] | Reserved | Always returns 000. |
| [4:0] | PMB_STATUS | Provides detail for the most recent PMBus transfer, which had a problem. A value of 0 indicates no recorded problem. Once set to a non-zero value, PMB_STATUS holds that value until another PMBus transfer has a problem. Table 38 details the code values. The register can also be written. Writing a non-zero value results on the status bit setting shown in Table 38. |

*Table 38. PMB_STATUS Detail*

| Value | Description | Target Bit |
|---|---|---|
| 0x01 | Chip busy due to previous command | STATUS:BUSY |
| 0x02 | Reserved | N/A |
| 0x03 | Incoming PEC bad | STATUS_CML:PEC_FAILED |
| 0x04 | Repeated start or stop bit received not on byte boundary | STATUS_CML:MISC_FAULT |
| 0x05 | Stop bit received before end, no PMBus error | N/A |
| 0x06 | Read was NACK'ed before final byte, no PMBus error | N/A |
| x0x7 | Host read too many bytes | STATUS_CML:MISC_FAULT |
| 0x08 | Host wrote too many bytes | STATUS_CML:BAD_DATA |
| 0x09 | Target address with R/W# high rejected | STATUS_CML:MISC_FAULT |
| 0x0A | Bad command code received | STATUS_CML:BAD_CMD |
| 0x0B | Attempt to write invalid data value | STATUS_CML:BAD_DATA |
| 0x0C | Attempt to write a read-only command | STATUS_CML:BAD_DATA |
| 0x0D | Reserved | N/A |
| 0x0E | Reserved | N/A |
| 0x0F | Reserved | N/A |
| 0x10 | Reserved | N/A |
| 0x11 | Reserved | N/A |
| 0x12 | Reserved | N/A |
| 0x13 | Byte count for block write incorrect | STATUS_CML:BAD_DATA |
| 0x14 | Reserved | N/A |
| 0x15 | Read data not available in time | STATUS:BUSY |
| 0x16 | SDAO data conflict (another chip pulled down SDA when data was coming from this chip) | STATUS_CML:MISC_FAULT |
| 0x17 | SDAO conflict specifically on ARA, no PMBus error | N/A |
| 0x18 | Reserved | N/A |
| 0x19 | Attempted read of write-only (TX-byte) command | STATUS_CML:MISC_FAULT |
| 0x1A | Reserved | N/A |
| 0x1B | Reserved | N/A |
| 0x1C | Reserved | N/A |
| 0x1D | Reserved | N/A |
| 0x1E | Reserved | N/A |
| 0x1F | Reserved | N/A |

## APPLICATIONS INFORMATION

*Table 39. MFR_PADS_LIVE_STATUS (0xE5) Read Only*

| Bit | Name | Operation |
|---|---|---|
| 15 | POWER_FAILED_STATUS | POWER_FAILED_STATUS is active when FB input pin goes below 2.56 V while the PG_LATCH status bit is set. That indicates a loss of output voltage after it was initially good. |
| 14 | FET_SHORT_STATUS | Indicates that the potential FET short if ($V_{SENSE+}$ – $V_{SENSE-}$) exceeds 2 mV while the external MOSFET is off, 1 = FET shorted, 0 = FET not shorted. |
| [13:12] | Reserved | Always returns 00. |
| 11 | Reserved | Reserved |
| 10 | GATE | Indicates that the state of GATE Pin, 1 = GATE Pin high, 0 = GATE Pin low. |
| 9 | TMR_LOW | Indicates that whether TMR Pin is Low, 1 = TMR is lower than 0.2 V, 0 = TMR is higher than 0.2 V. |
| 8 | PG_LATCH | Latched signal is active when system power seems good. The conditions to set are FB > 2.56 V, $V_{GS}$ > 8V, and $V_{DS}$ < 2 V. Either FB low or external MOSFET turned off clears PG_LATCH depending on the PWRGD_RESET bit. |
| 7 | EN_INPUT | Bit is 1 to indicate that the EN pin is in the active state. |
| 6 | IOUT_OC_STATUS | Overcurrent condition from comparator, 1 = Overcurrent, 0 = not overcurrent. |
| 5 | VIN_UV_STATUS | Indicates that the input undervoltage when UV pin is low, 1 = UV low, 0 = UV high. |
| 4 | VIN_OV_STATUS | Indicates that the input overvoltage when OV pin is high, 1 = OV high, 0 = OV low. |
| 3 | OP1_STATUS | Bit is 1 to indicate that the $P_{IN}$ is exceeding the MFR_PIN_OP1_FAULT_LIMIT value. The bit automatically clears when $P_{IN}$ falls below that value. |
| 2 | FET_BAD_STATUS | Indicates that the FET Bad condition is present, 1 = FET Bad condition present, 0 = FET Bad condition not present. |
| 1 | Reserved | Reserved |
| 0 | Reserved | Reserved |

*Table 40. MFR_COMMON (0xEF) Read Only*

| Bit | Name | Default | Operation |
|---|---|---|---|
| 7 | ALERT_LATCH# | 1 | Bit is 0 when the 4286 is pulling down ALERT#. |
| 6 | PMB_BUSY# | 1 | Bit is 0 when some registers are unavailable for PMBus access. |
| [5:4] | Reserved | 11 | Always returns 11. |
| 3 | Reserved | 0 | Reserved |
| [2:0] | Reserved | 110 | Always returns 110. |

*Table 41. MFR_SD_CAUSE (0xF1) Read Only*

| Bit | Name | Default | Operation | |
|---|---|---|---|---|
| [7:4] | Reserved | 0000 | Always returns 0000. | |
| [3:0] | HS_SHUTDOWN_CAUSE | 0000 | Cause of last hot-swap shut down. | |
| | | | **HS_SHUTDOWN_CAUSE[3:0]** | **Cause** |
| | | | 0001 | OPERATION command |
| | | | 0010 | EN pin |
| | | | 0011 | REBOOT or restart |
| | | | 0100 | INTVCC_UVLO |
| | | | 0101 | TSD (thermal shut down) |
| | | | 0110 | VDD_UVLO |
| | | | 0111 | OT_FAULT |
| | | | 1000 | IOUT_OC_FAULT |
| | | | 1001 | PIN_OP2_FAULT |
| | | | 1010 | PIN_OP1_FAULT |
| | | | 1011 | FET_BAD_FAULT |
| | | | 1100 | VIN_UV_FAULT |
| | | | 1101 | VIN_OV_FAULT |

## APPLICATIONS INFORMATION

*Table 41. MFR_SD_CAUSE (0xF1) Read Only (Continued)*

| Bit | Name | Default | Operation | |
|---|---|---|---|---|
| | | | 1110 | Reserved |
| | | | 1111 | Reserved |

*Table 42. MFR_CONFIG1 (0xF2) R/W*

| Bit | Name | Default | Operation | |
|---|---|---|---|---|
| 15 | Reserved | 0 | Always returns 0. | |
| 14 | Reserved | 1 | Reserved, always write 1. | |
| [13:10] | ILIM | 0101 | Configures the sense reference voltage for current limit, see Table 5. Configuring current-limit with the ISET pin. | |
| [9:8] | Reserved | 01 | Reserved, always write 01. | |
| 7 | Reserved | 0 | Always returns 0. | |
| [6:5] | Reserved | 11 | Reserved, always write 11. | |
| [4:2] | Reserved | 100 | Reserved, always write 100. | |
| 1 | VRANGE_SELECT | 1 | Selects a voltage range for $V_{IN}$ and $V_{OUT}$ measurements. | |
| | | | **VRANGE_SEL** | **Voltage Range for $V_{IN}$ and $V_{OUT}$** |
| | | | 0 | 25.6 V |
| | | | 1 | 102.4 V |
| 0 | VPWR_SELECT | 0 | Selects voltage for power multiplication (optional). See VIN_VOUT_SELECT bit for interaction with ADC auxiliary input list. | |
| | | | **VPWR_SELECT** | **Voltage for Power Multiplication** |
| | | | 0 | $V_{IN}$ (attenuated $V_{DD}$ voltage for input power.) |
| | | | 1 | $V_{OUT}$ (attenuated SOURCE voltage for FET power.) |

*Table 43. MFR_CONFIG2 (0xF3) R/W*

| Bit | Name | Default | Operation |
|---|---|---|---|
| [15:14] | Reserved | 00 | Always returns 00. |
| 13 | Reserved | 0 | Reserved, always write 0. |
| 12 | SEL_1M | 0 | Set bit to enable 1 Mbit-compatible timing for PMBus. |
| [11:10] | Reserved | 00 | Reserved, always write 00. |
| [9:8] | Reserved | 00 | Reserved, always write 00. |
| 7 | RESET_FAULT_ENABLE | 1 | Enables fault reset on an edge of the EN pin going active. 1 = EN active edge resets fault register bits, 0 = EN active edge has no impact on fault register bits |
| 6 | PWRGD_RESET_ CNTRL | 1 | Configures PG_LATCH Reset, 1 = FB Low Resets PG_LATCH, 0 = FET Off Resets PG_LATCH. |
| 5 | MASS_WRITE_ ENABLE | 1 | Enables mass Write or global address to this device and others on the SMBus, 1 = Mass Write Enabled, 0 = Mass Write Disabled. |
| 4 | Reserved | 0 | Always returns 0. |
| 3 | Reserved | 1 | Reserved, always write 1. |
| 2 | EXT_TEMP_ENABLE | 1 | Enables the use of an external temperature sensor on GPIO3 (default), falls back to on-chip temperature sensor when disabled. |
| 1 | DB_EN_ON_EN | 1 | Enables use of debounce timer for EN transitions. |
| 0 | Reserved | 1 | Reserved, always write 1. |

## APPLICATIONS INFORMATION

*Table 44. MFR_GPIO_INV (0xF4) R/W*

| Bit | Name | Default | Operation |
|---|---|---|---|
| [15:10] | Reserved | 000000 | Reserved for future use, write 0 only. |
| 9 | RBT_INV | 0 | Assigns polarity for GPIO input associated with reboot input, 0 = rising edge of GPIO pin triggers reboot (REBOOT input), 1 = falling edge of GPIO pin triggers reboot (REBOOT# input). |
| 7 | INV8 | 1 | Assigns polarity for GPIO8 output, 0 = GPIO8 pin pulls low when specified output bit is low, 1 = GPIO8 pin pulls low when specified output bit is high. |
| 6 | INV7 | 0 | Assigns polarity for GPIO7 output, 0 = GPIO7 pin pulls low when specified output bit is low, 1 = GPIO7 pin pulls low when specified output bit is high. |
| 5 | INV6 | 0 | Assigns polarity for GPIO6 output, 0 = GPIO6 pin pulls low when specified output bit is low, 1 = GPIO6 pin pulls low when specified output bit is high. |
| 4 | INV5 | 1 | Assigns polarity for GPIO5 output, 0 = GPIO5 pin pulls low when specified output bit is low, 1 = GPIO5 pin pulls low when specified output bit is high. |
| 3 | INV4 | 1 | Assigns polarity for GPIO4 output, 0 = GPIO4 pin pulls low when specified output bit is low, 1 = GPIO4 pin pulls low when specified output bit is high. |
| 2 | INV3 | 0 | Assigns polarity for GPIO3 output, 0 = GPIO3 pin pulls low when specified output bit is low, 1 = GPIO3 pin pulls low when specified output bit is high. |
| 1 | INV2 | 1 | Assigns polarity for GPIO2 output, 0 = GPIO2 pin pulls low when specified output bit is low, 1 = GPIO2 pin pulls low when specified output bit is high. |
| 0 | INV1 | 1 | Assigns polarity for GPIO1 output, 0 = GPIO1 pin pulls low when specified output bit is low, 1 = GPIO1 pin pulls low when specified output bit is high. |

## APPLICATIONS INFORMATION

### GPIO OUTPUT SELECTION

*Table 45. Output Selection*

| SELn[3:0][1] | Output |
|---|---|
| 0000 | Three-state |
| 0001 | MFR_GPO_DATA[n−1] |
| 0010 | CMPOUT |
| 0011 | PWR_GOOD |
| 0100 | FAULT |
| 0101 | IOUT_OC_STATUS |
| 0110 | Reserved |
| 0111 | Reserved |
| 1000 | OP1_STATUS |
| 1001 | ALERT |
| 1010 | L_ALERT |
| 1111 | Temperature Sensor (GPIO3 only) |

[1] This table is common to all eight GPIO pins with n to be replaced by the GPIO number (1 to 8).

*Table 46. MFR_GPO_SEL_41 (0xF5) R/W*

| Bit | Name | Default | Operation |
|---|---|---|---|
| [15:12] | SEL4[3:0] | 0101 | Selects a GPIO4 output. |
| [11:8] | SEL3[3:0] | 1111 | Selects a GPIO3 output. |
| [7:4] | SEL2[3:0] | 0100 | Selects a GPIO2 output. |
| [3:0] | SEL1[3:0] | 0011 | Selects a GPIO1 output. |

*Table 47. MFR_GPO_SEL85 (0xF6) R/W*

| Bit | Name | Default | Operation |
|---|---|---|---|
| [15:12] | SEL8[3:0] | 1000 | Selects a GPIO8 output. |
| [11:8] | SEL7[3:0] | 0010 | Selects a GPIO7 output. |
| [7:4] | SEL6[3:0] | 0000 | Selects a GPIO6 output. |
| [3:0] | SEL5[3:0] | 0111 | Selects a GPIO5 output. |

*Table 48. MFR_GPI_SEL (0xF7) R/W*

| Bit | Name | Default | Operation | |
|---|---|---|---|---|
| [15] | Reserved | 0 | Always returns 0. | |
| [14:12] | Reserved | 000 | Reserved for future use, write 000 only. | |
| 11 | Reserved | 0 | Reserved for future use, write 0 only. | |
| [10:8] | Reserved | 000 | Reserved for future use, write 000 only. | |
| 7 | RBT_EN | 0 | This bit enables a GPIO pin (configured as REBOOT# or REBOOT) to generate a reboot, turns off the power MOSFETs, waits a programmed delay of 0.5 s to 68 s, and then restarts the MOSFETs to power cycle the load. Optionally, chip reset may occur during the turn-off period. | |
| [6:4] | RBT_SEL [2:0] | 000 | Selects a GPIO pin as a reboot trigger (REBOOT# or REBOOT) input. | |
| 3 | Reserved | 0 | Always returns a 0. | |
| [2:0] | CMP_SEL [2:0] | 101 | **CMP_SEL[2:0]** | **Input** |
| | | | 000 | GPIO1 |
| | | | 001 | GPIO2 |
| | | | 010 | GPIO3 |
| | | | 011 | GPIO4 |
| | | | 100 | GPIO5 |

## APPLICATIONS INFORMATION

*Table 48. MFR_GPI_SEL (0xF7) R/W (Continued)*

| Bit | Name | Default | Operation | |
|---|---|---|---|---|
| | | | 101 | GPIO6 |
| | | | 110 | GPIO7 |
| | | | 111 | GPIO8 |

*Table 49. MFR_REBOOT_CONTROL (0xFD) R/W*

| Bit | Name | Default | Operation |
|---|---|---|---|
| [7:6] | Reserved | 00 | Always returns 00. |
| [5:4] | RBT_INIT | 00 | Selects chip initialization options following the reboot:<br>00 = chip is reset.<br>01 = chip is reset.<br>10 = no reset. FETs are turned off and then back on after the auto reboot turn-on delay that follows these bits. |
| 3 | REBOOT | 0 | Write a 1 to reboot. This bit is not cleared by the reboot operation so software can check that a reboot just took place. |
| [2:0] | Reserved | 000 | Reserved. |

## TYPICAL APPLICATION

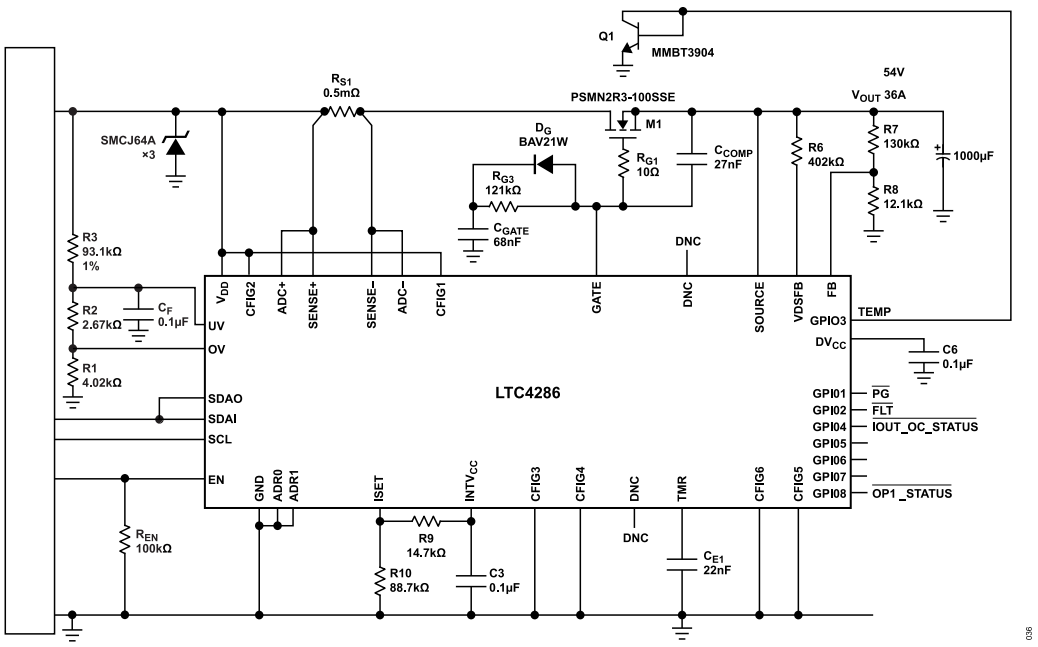


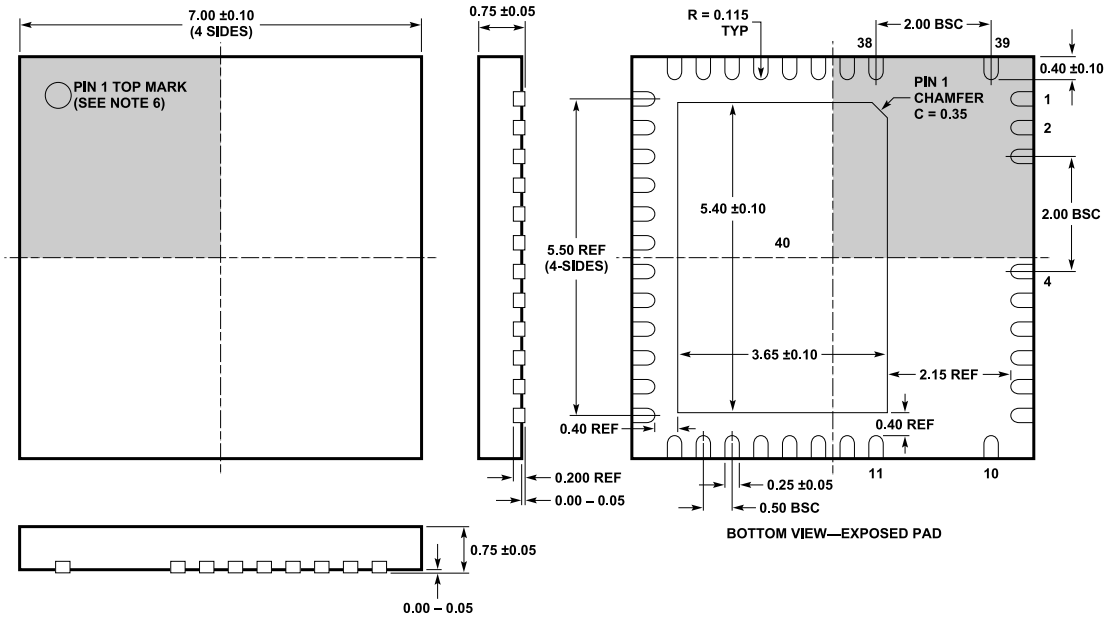

*Figure 35. LTC4286 Typical Application*

## RELATED PARTS

*Table 50. Related Part Numbers*

| Part Number | Description | Comments |
|---|---|---|
| LTC4260 | Positive high voltage hot-Swap controller with I²C compatible monitoring | 8-bit ADC monitoring current and voltages, supplies from 8.5 V to 80 V, single MOSFET driver. |
| LTC4238 | High voltage high current hot-swap controller | Operates from 6.5 V to 80 V, compatible with LTC4286 with COMM/GPIO5 pins, dual MOSFET drivers. |
| ADM1272 | High voltage positive hot-swap controller and digital power monitor with PMBus | Operates from 16 V to 80 V, single MOSFET driver. |
| LTC4282 | High current hot-swap controller with I²C compatible monitoring | Operates from 2.9 V to 33 V, 12-bit ADC monitoring current, voltage, and power, dual MOSFET drivers. |

## OUTLINE DIMENSIONS




NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WKKD-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

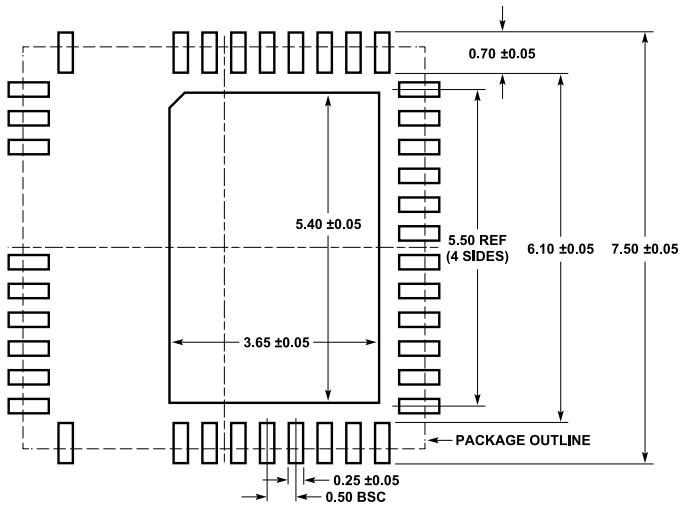



*Figure 36. 48(39)-Lead Plastic QFN (7 mm × 7 mm)*
*(05-08-1792)*
*Dimensions shown in millimeters*

## OUTLINE DIMENSIONS

Updated: December 13, 2022

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Description | Packing Quantity | Package Option |
|---|---|---|---|---|
| LTC4286AUK#PBF | −40°C to +125°C | 48(39)-Lead Plastic QFN (7 mm x 7 mm x 0.75 mm with EPAD) | | 05-08-1792 |
| LTC4286AUK#TRPBF | −40°C to +125°C | 48(39)-Lead Plastic QFN (7 mm x 7 mm x 0.75 mm with EPAD) | Reel, 2000 | 05-08-1792 |

[1] All models are RoHS compliant.

## EVALUATION BOARDS

| Model[1] | Description |
|---|---|
| EVAL-LTC4286-A1Z | Evaluation Board |

[1] Z = RoHS Compliant Part.

$I^2C$ refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).